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Issue 25/2007

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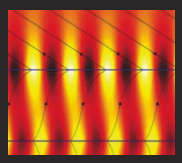

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ROBOTS ON THE MARCH

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PHASE STEPS OVERCOME SLIM TESTING MARGINS

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RADIO + MCU + FLASH + USB

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The new **CC1111** from Texas Instruments is the first sub-1 GHz RF SoC with an integrated full-speed USB controller, enabling a fast and easy bridge between PCs and RF. The integration of a high-performance radio, MCU, Flash memory and USB controller results in smaller PCB size, easier assembly and reduced overall system cost. Combined with TI's SimpliciTI™ network protocol, the CC1111 provides easy development and improved low-power design.

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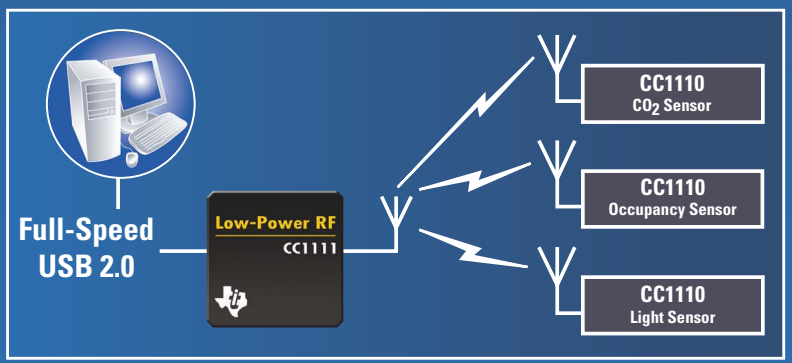

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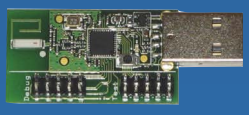

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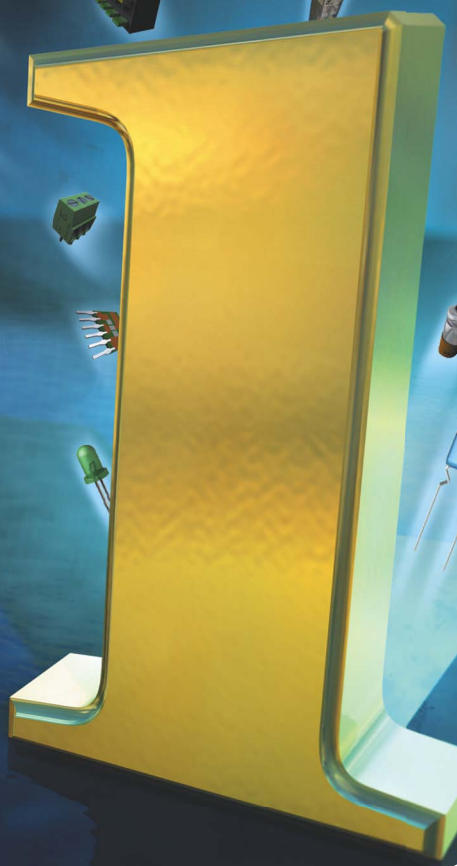

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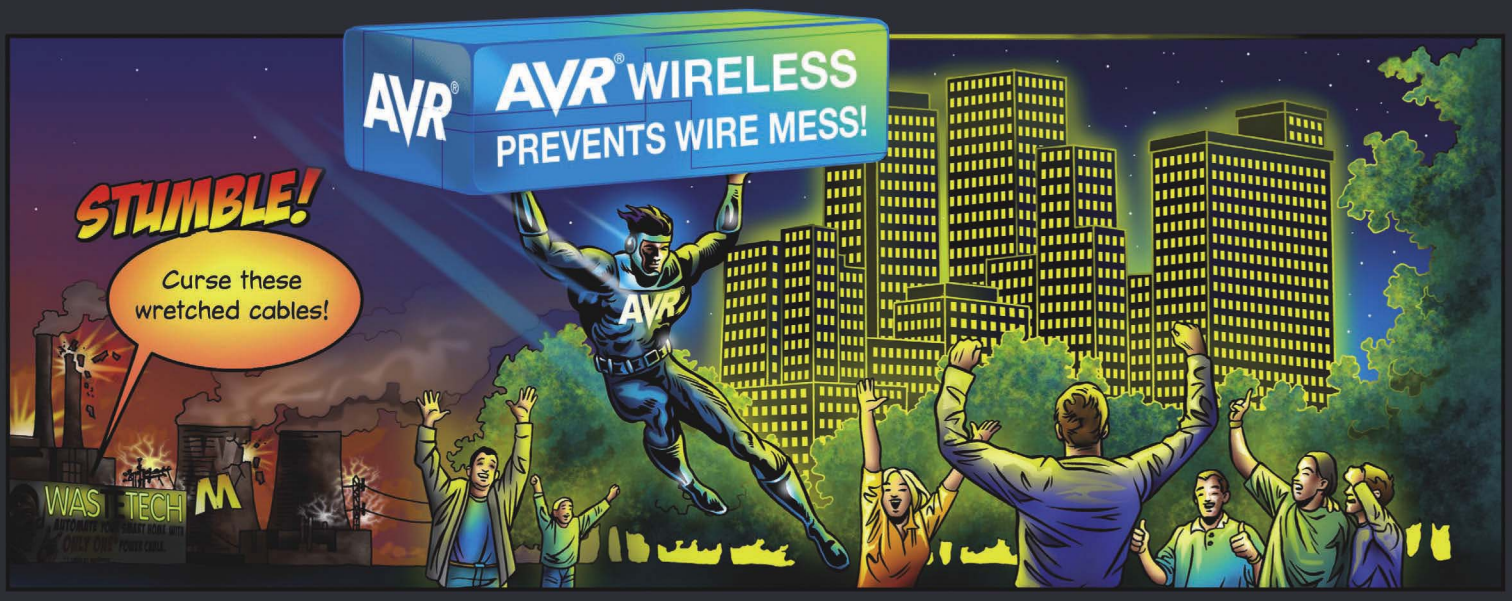

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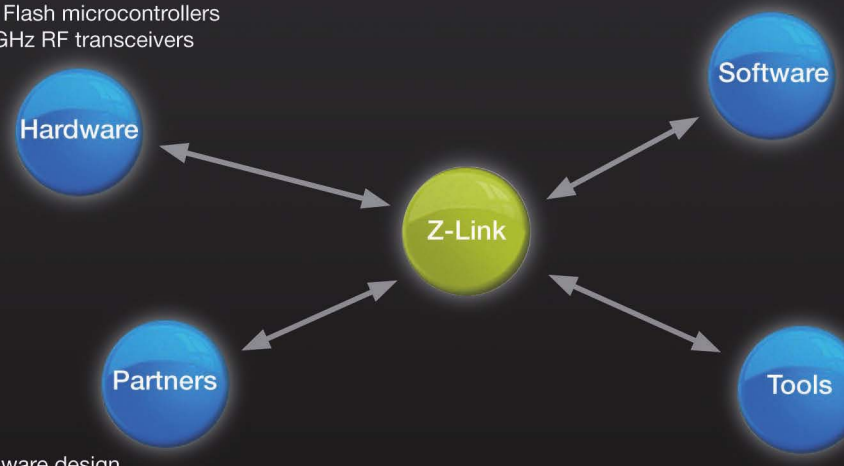

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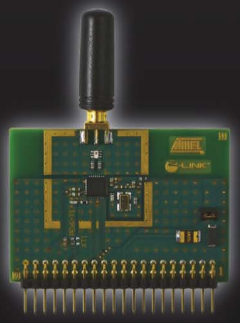

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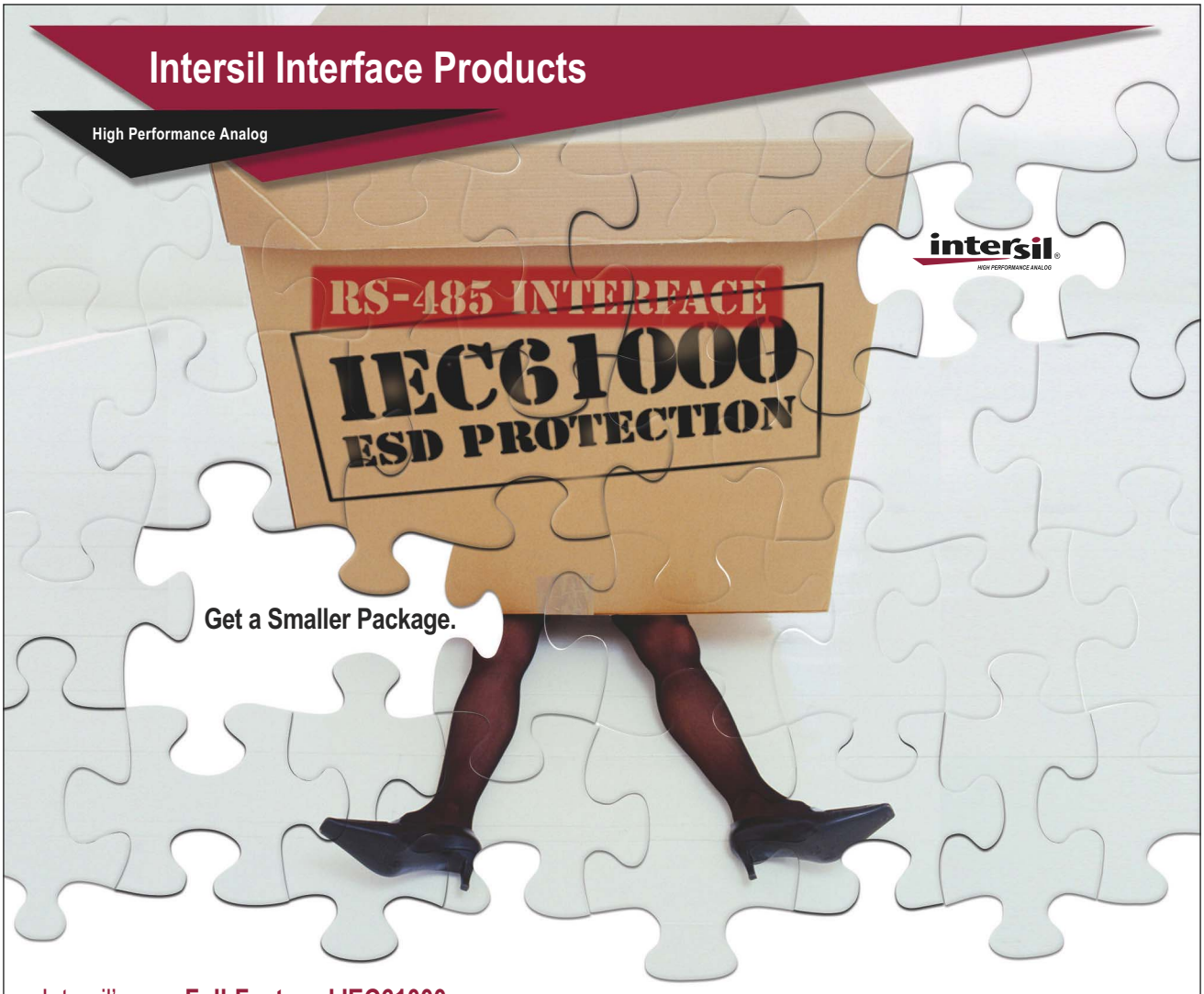

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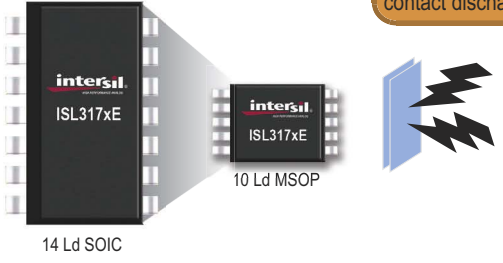

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ISL317xE Key Features:

- Full fail-safe for predictable performance when bus faults occur.
- Hot Plug capability prevents data corruption during power-up on an active bus.
- Fractional unit load (allows up to 256 devices on the bus).

Device	Data Rate (Mbps)	Slew Rate Limited	Tx/Rx Enable	Package
ISL3170E	0.25	Yes	Yes	10 Ld MSOP, 14 Ld SOIC
ISL3171E	0.25	Yes	No	8 Ld MSOP, 8 Ld SOIC
ISL3172E	0.25	Yes	Yes	8 Ld MSOP, 8 Ld SOIC
ISL3173E	0.5	Yes	Yes	10 Ld MSOP, 14 Ld SOIC
ISL3174E	0.5	Yes	No	8 Ld MSOP, 8 Ld SOIC
ISL3175E	0.5	Yes	Yes	8 Ld MSOP, 8 Ld SOIC
ISL3176E	20	No	Yes	10 Ld MSOP, 14 Ld SOIC
ISL3177E	20	No	No	8 Ld MSOP, 8 Ld SOIC
ISL3178E	20	No	Yes	8 Ld MSOP, 8 Ld SOIC

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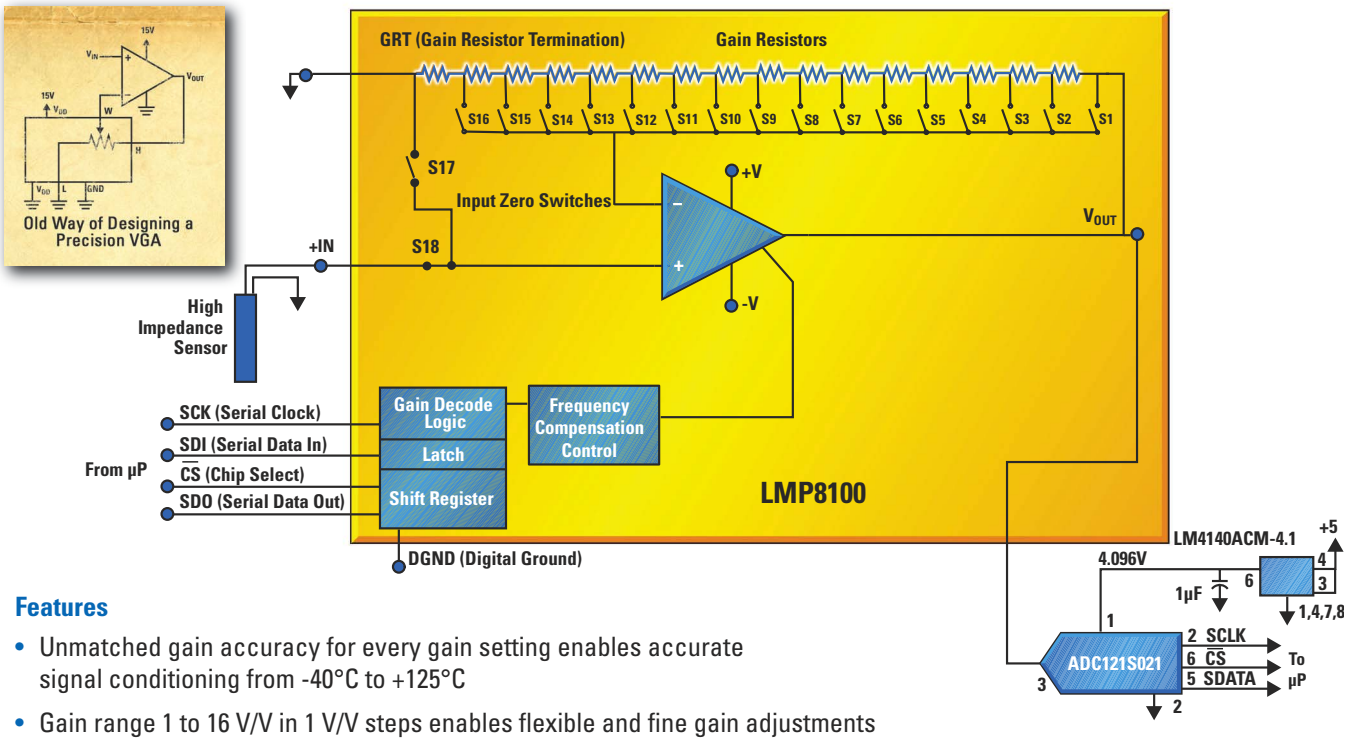

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- Gain range 1 to 16 V/V in 1 V/V steps enables flexible and fine gain adjustments
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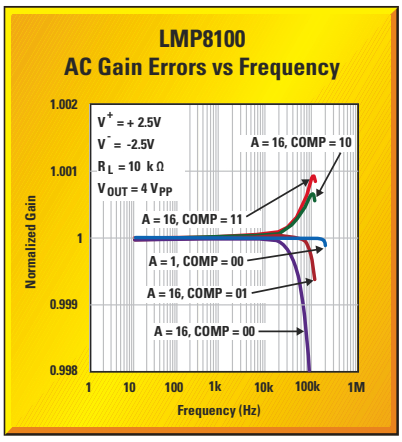
Ideal for use in industrial instrumentation, sensor interface, data acquisition, test equipment, and gain control applications



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The Sight & Sound of Information

EDN contents

12.3.07

Robots on the march

 Robotics is gaining momentum as an engineering discipline. A variety of available platforms and tools supports it. This article is the first of a two-part hands-on project exploring the topic.

by Robert Cravotta, Technical Editor

Phase steps overcome slim testing margins

 With a new multiple-strobe technique, your ATE can find the passing setup-and-hold margins during high-volume production testing of source-synchronous circuits.

by Stefan Walther and Guido Schulze, Verigy

Coding SPI software

 The SPI requires three wires for data transfer plus a device-select signal. Designers can implement peripheral communications using processor-based hardware or the software routines that this article presents.

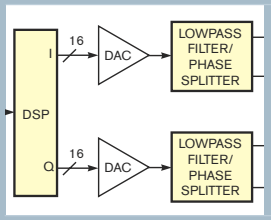
by Dariusz Caban, PhD, Silesian University of Technology

Decompensating amplifiers improve performance

 Manufacturers offering unity-gain-stable amplifiers hope to address a wide market and minimize the effort of learning to use the devices. Yet these vendors sacrifice a significant portion of the potential ac performance. Learn when to consider decompensated amplifiers and what they can offer you.

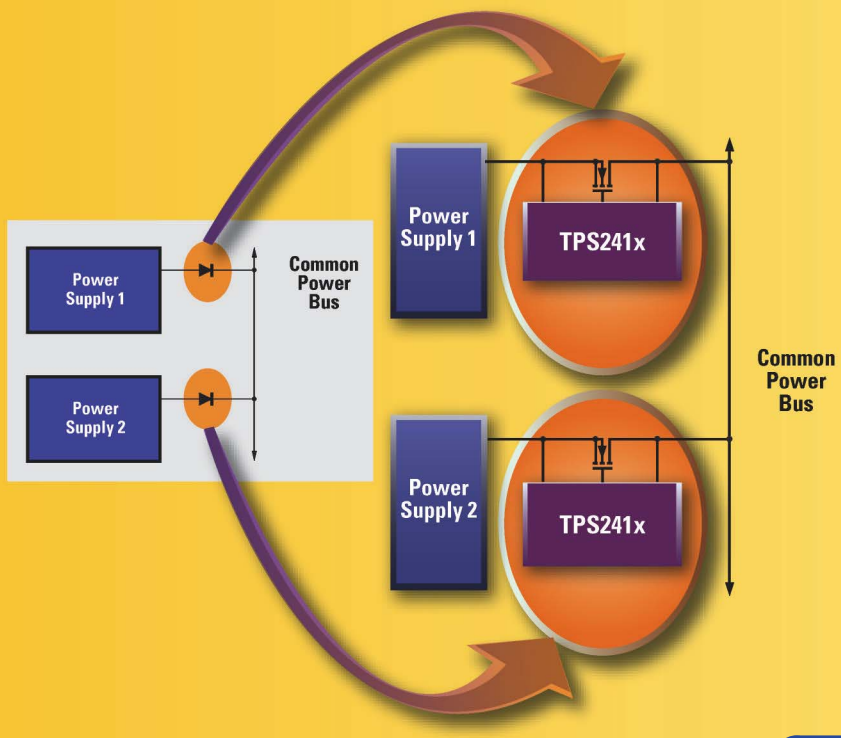
by Walter Bacharowski, National Semiconductor

DESIGNIDEAS



ORing FET Controllers Save Power

Protect Redundant Power Supply Systems



Applications

- Blade servers
- N+I redundant systems
- Telecom line cards
- RAID
- Merchant power

Features

- Ultra-fast, adjustable gate turn-off
- Internal charge pump
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- Adjustable turn-off threshold
- Complements TI's TPS2490 hot swap controller

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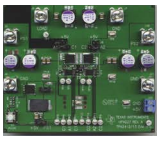
The new **TPS241x** family of ORing controllers from Texas Instruments provides a high-efficiency replacement for ORing diodes. Also, they offer intelligent monitoring and control of power supplies to prevent bus transient events from causing board-damaging faults or voltage spikes during operation. These ICs provide 130ns ultra-fast gate turnoff and a wide voltage operation range from 16.5V down to 0.8V.

Device	Linear Gate Control	On/Off Gate Control	Fast Comparator Filtering	Voltage Monitoring	MOSFET Fault Monitoring	Enable Control	Status Pin	Package
TPS2410	X		X	X	X	X	X	14-Pin TSSOP
TPS2411		X	X	X	X	X	X	14-Pin TSSOP
TPS2412	X							8-Pin TSSOP
TPS2413		X						8-Pin TSSOP



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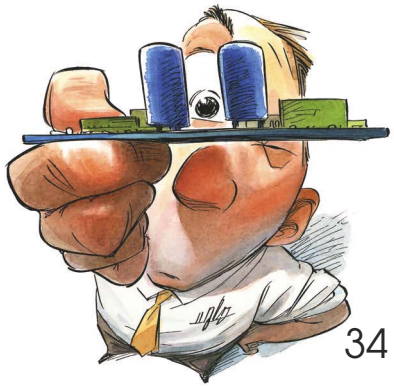

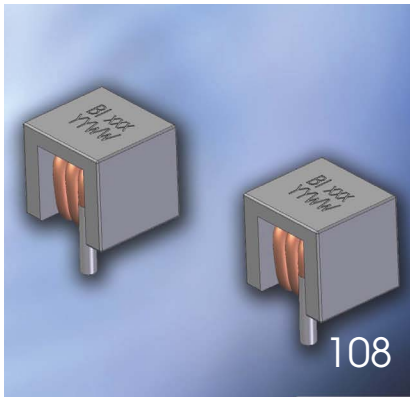

DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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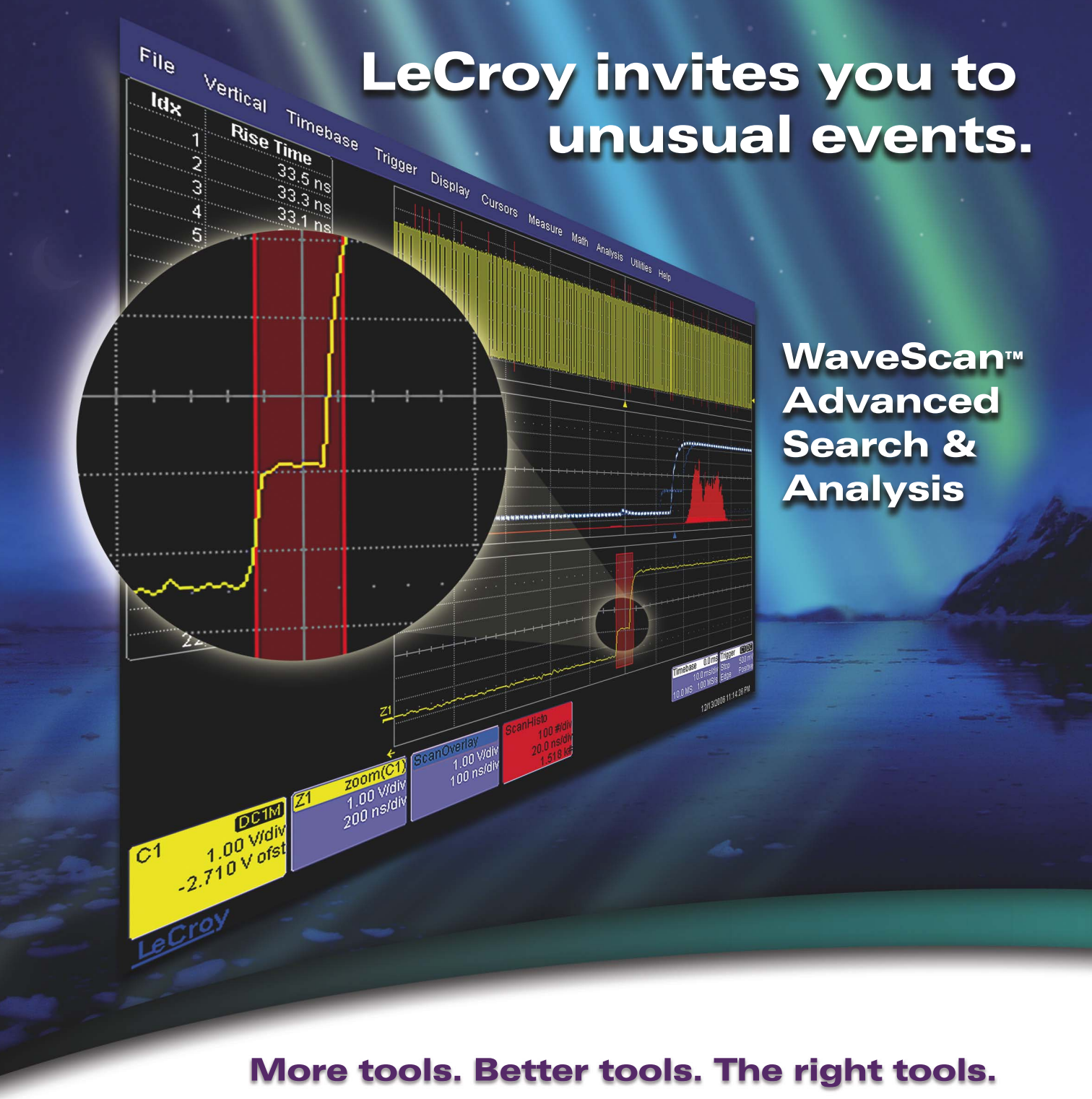

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EDN Magazine has included LeCroy's WaveRunner® Xi and WaveSurfer® Xs with WaveScan in it's 'Hot 100 Products' list. WaveScan is also an EDN 2007 Innovation Award Finalist.

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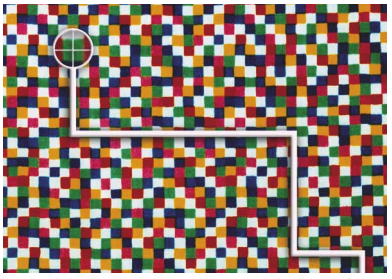

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Check out these Web-exclusive articles

The need for local search in embedded consumer devices
As the available memory in portable embedded devices grows, designers are investigating low-impact data-management techniques to tag, store, locate, and retrieve local information.
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Hynix touts 1-Gbit GDDR5 DRAM
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Qualcomm moves 3G chips to 45-nm process
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Roles shift as the embedded-systems design chain disaggregates
→www.edn.com/article/CA6497064

Synopsys releases design-to-mask data-processing tool for TSMC's advanced process nodes
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The MathWorks adds support for parallel-apps, multithreaded computations, 64-bit platforms
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Intel formally debuts 45-nm Penryn processors
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CMOS running out of gas, new effort looks for scalable replacement
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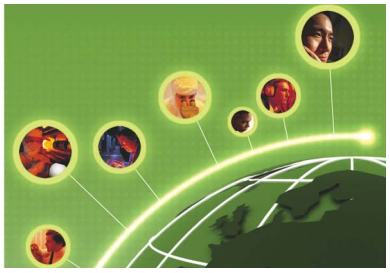

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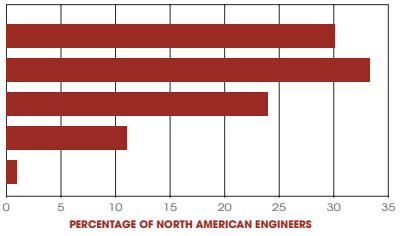

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FROM *EDN*'S BLOGS
65-nm adoption is slow and fraught with issues
From *Practical Chip Design*
by Ron Wilson
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→www.edn.com/071203toc5

MICROPROCESSOR DIRECTORY
The 34th annual microprocessor directory delivers architecture descriptions for hundreds of devices and cores, block diagrams, and voluminous specification tables. The online tool allows you to drill down by vendor or target application to quickly identify candidate processors for your projects.
→www.edn.com/microdirectory

BY MAURY WRIGHT, EDITORIAL DIRECTOR

Development boards speed learning and product-development cycle

I suppose the headline is a no-brainer. Of course, development boards help you come up to speed on a new technology. And the boards can jump-start a project, allowing you, for instance, to immediately start software development while you contemplate a custom hardware design. A UK sister publication, *Electronics Weekly*, recently researched development boards and uncovered some points that you might find interesting. I'd like to ask you readers in North America some of the same questions.

The magazine fielded the survey primarily to design and development engineers. The survey asked engineers how often they searched for information about development boards. A third of the respondents reported searching once a month, 11% search every week, and 2% search every day. Those figures mean that almost 50% of the respondents search at least monthly, and another 31% search once every six months. Ironically, the respondents didn't report using development boards as often as they searched. Only 20% reported using a development board at least monthly.

Electronics Weekly also asked when in the course of a project the engineers were most likely to look for development boards. The second and third most prevalent responses are no surprise: 40% reported searching for development boards during prototyping, and 49% reported searching during concept development. I was surprised at the No. 1 answer: 53% reported searching during basic research. To me, that percentage implies that engineers use development boards more as educational tools than as development tools.

Should *EDN* spend more time and energy on spotlighting development boards?

The survey also asked about the usefulness of a number of resources in searching for development boards. Google and vendor Web sites topped the list at 62 and 59%, respectively, with "very useful" ratings—no surprise there. The news for trade publications, such as *EDN*, was less promising: Only 7% found our Web sites very useful in looking for such boards. The results make me wonder whether *EDN* should spend more time and energy on spotlighting development boards. We regularly mention such boards, especially when manufacturers launch them as development vehicles for new ICs, but we haven't lately focused articles or directories on development boards. I was also surprised that only 18% of the respondents found distributor Web sites useful in searching for development boards because distributors have a lot of development boards available.

The survey also asked a simple question about the type of development boards engineers use: general-purpose or application-specific units. A majority—59%—use general-purpose boards with microprocessors, I/O, displays, and other features. The remaining 41% use boards specific to functions, such as motion control, power supplies, and wireless networks.

Electronics Weekly asked why the engineers used development boards. Respondents weren't limited to a single answer and had to choose among the answers "strongly agree," "agree slightly," "disagree slightly," and "disagree strongly." At the top, 71% strongly agreed with "to quickly build a prototype," and 69% also strongly agreed with "to prove a concept." The response to the choice "to learn a new skill" conflicts with my earlier guess that the response would point toward educational usage. Only 32% strongly agreed with the new-skill choice, although 50% agreed slightly.

Finally, the survey asked where design engineers buy development boards. Respondents chose the distributor channel as No. 1 at 76%, despite the fact that respondents gave distributors low scores as resources for searching for boards. Purchasing boards directly from manufacturers was the second choice at 74%.

So, how do you use development boards? What actions should *EDN* take to assist you? What development-board resources should we offer? Go to the online version of this article at www.edn.com/071203ed, complete our survey on development-board usage, and you'll enter a drawing for a special development prize. EDN

Contact me at mgwright@edn.com.

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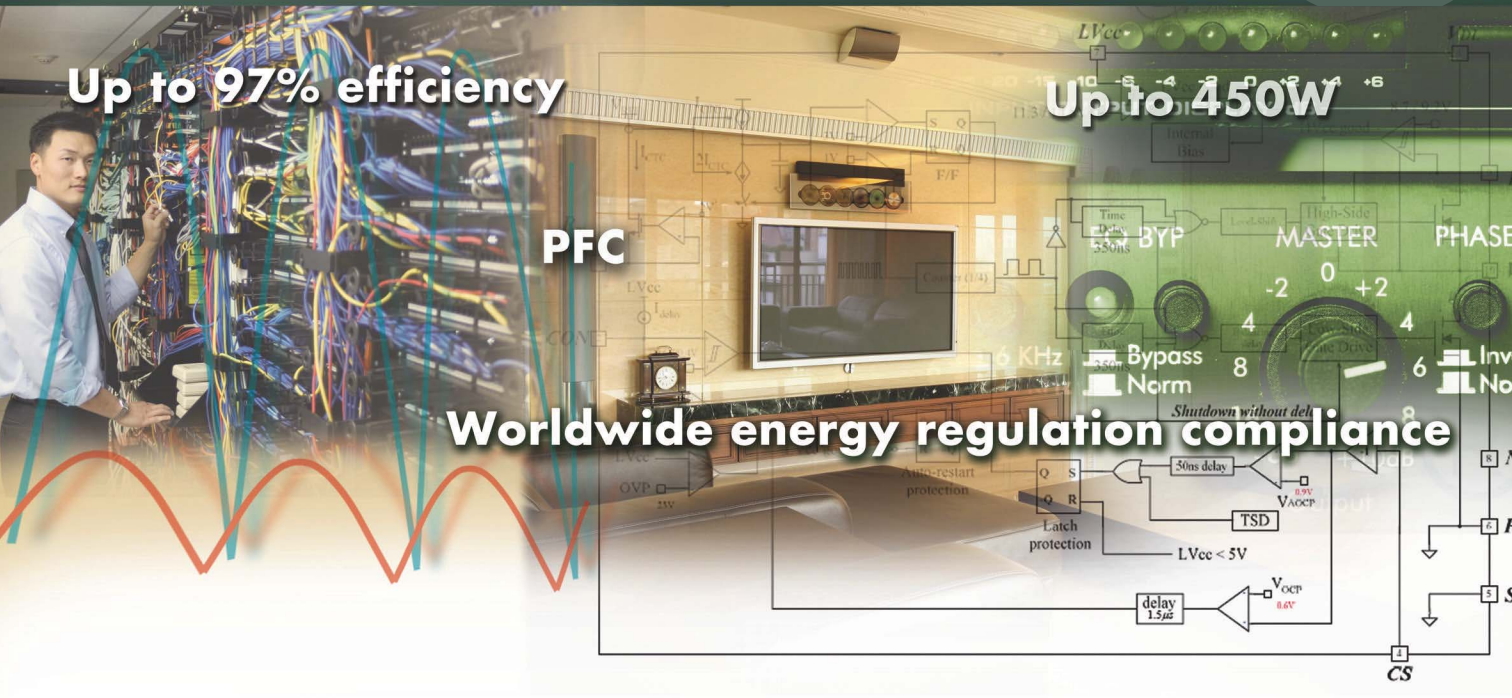

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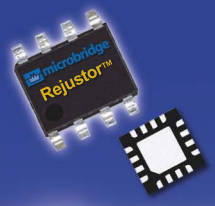

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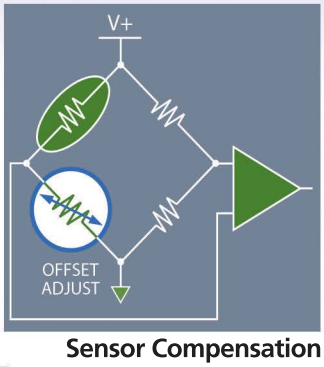
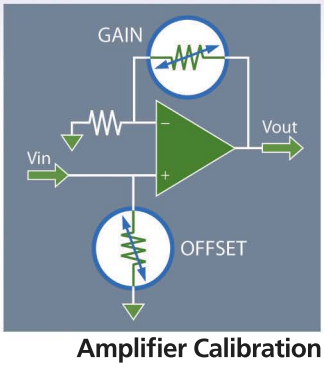


Sensor Compensation



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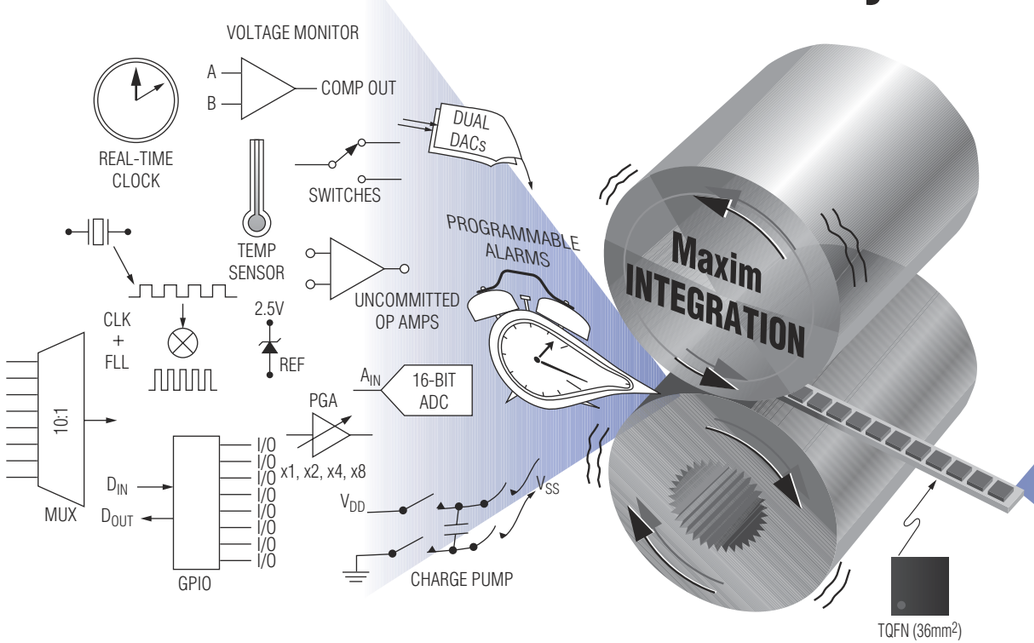

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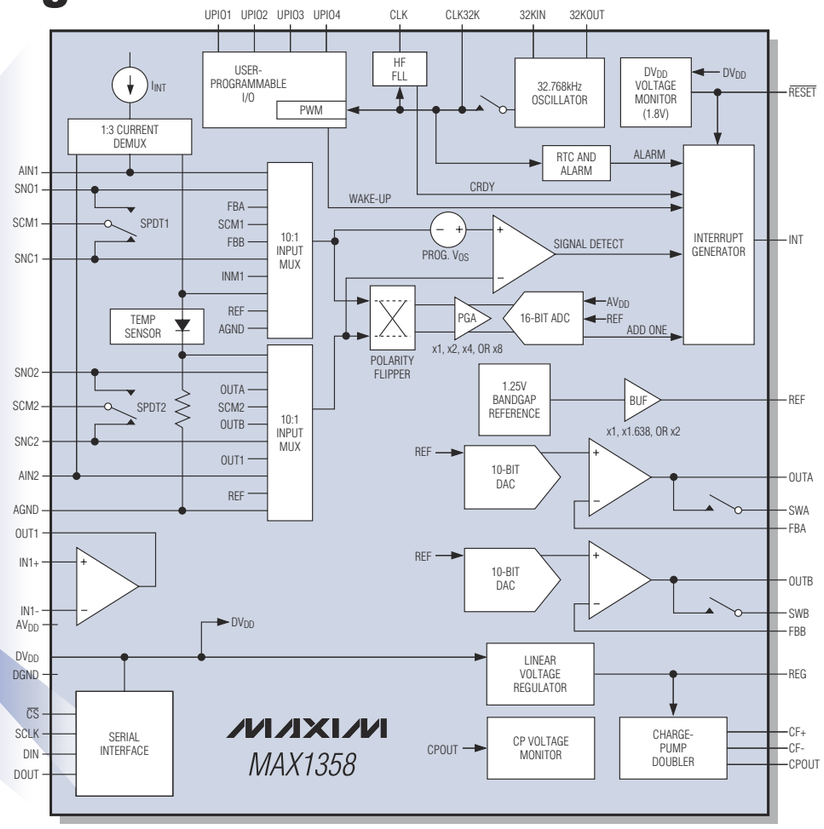

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MAX1360*	16-bit, sigma delta	2	0.01 to 0.512	0	3	4	2/0

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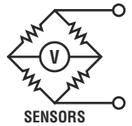

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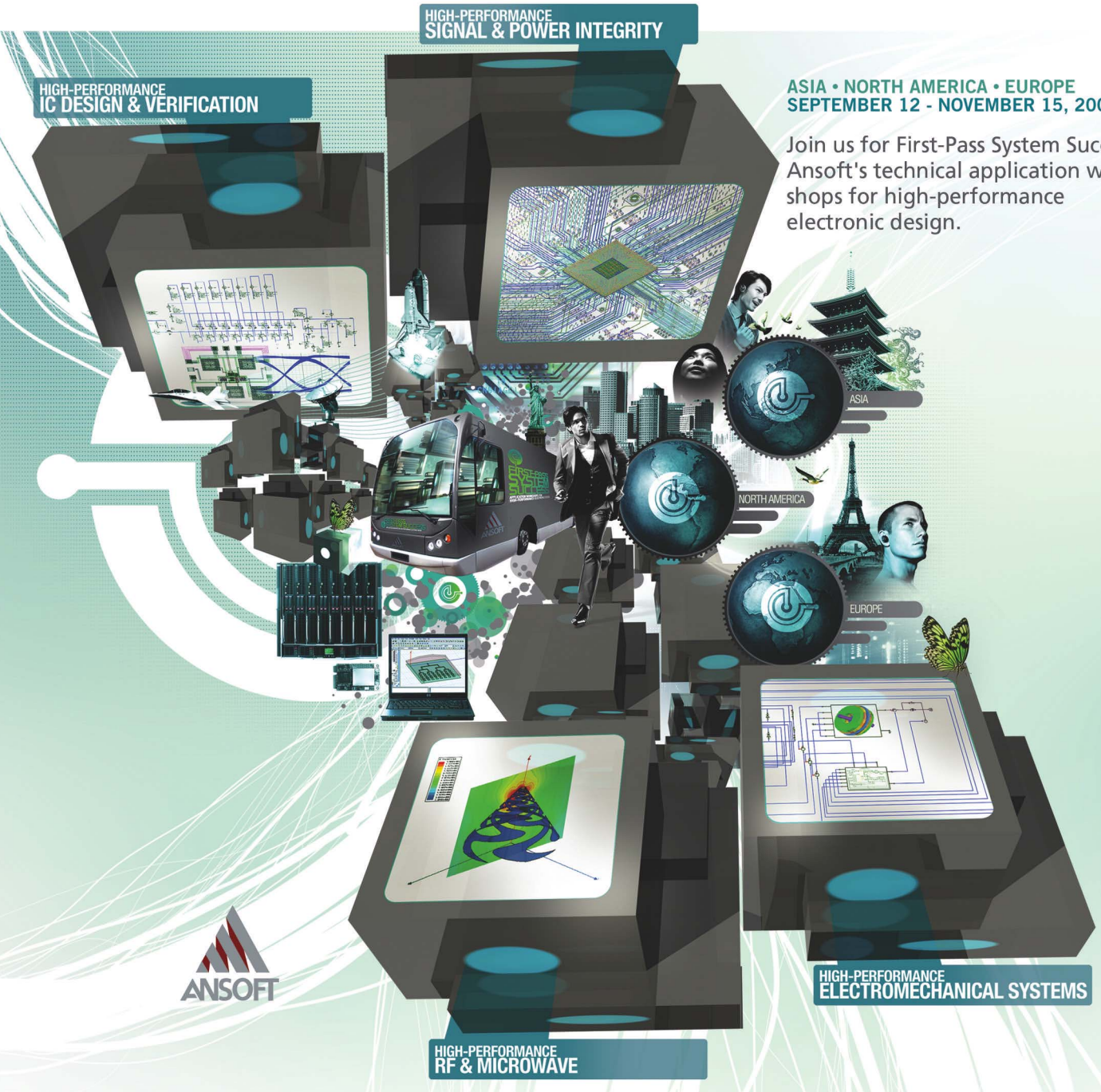

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Using Self-Calibration to Improve Performance of Ultra High-Speed Data Converters

Application Note AN-1727

Robbie Shergill, Applications

The ADC08xxxx family of Giga Sample Per Second (GSPS) A/D Converters (ADCs), incorporates sophisticated self-calibration circuitry. This application note gives the system designer a comprehensive description of how to use this feature. The device datasheets contain specific details about the self calibration features.

The Self-Calibration Scheme

Since calibration is essential to performance, the device performs self-calibration upon each power-up. In addition, the device allows the user to manually command the device to perform self-calibration as required. Typically this would be done when the system temperature has changed beyond a threshold that system design has established. Since ultimately it is the device's own temperature that affects its performance, an on-chip diode can be connected to an external temperature sensor for device temperature monitoring. National recommends the LM95221 temp sensor for this purpose.

The calibration procedure takes roughly 1–2 msec to complete, depending upon the CLK frequency and the specific device (refer to the device datasheet). In addition, at power-up only, the device inserts a much longer delay before starting the self-calibration process. This delay can be relatively short (tens of milliseconds) or relatively long (few seconds) and is user-selectable. The purpose of this delay is to allow the power-supply and other variables to stabilize. Also, when the device is configured in extended control mode the longer delay is not available (i.e. configured through the serial interface).

The CalRun pin always indicates whether the device is in self calibration mode or operating normally.

Performing Self-Calibration

Self-calibration is part and parcel of the "normal" operation of the device. As such, the device's operating conditions should be as stable and as close to "normal" system conditions as possible during calibration. The power supply, temperature and all inputs must be within the operating conditions stated in the datasheet and stable. Then, for greater calibration accuracy, the operating conditions should be as close to their operational state as possible.

In order to allow the conditions to stabilize, a certain amount of time delay would be necessary. The system engineer must decide what this time delay is for their system — which may vary from about 1–2 seconds to 10s of seconds. If longer delay is required then the CAL input pin can be used to further delay the start of the calibration cycle. The user does this by holding the CAL pin high during power up and keeping it high for as long a delay as desired. The device will wait until the CAL pin is cycled low and then high again before initiating the power-up calibration cycle.

The CAL input "low-then-high cycle" timing requirements can be found in the AC Electrical Characteristics table in the datasheet. Other than inhibiting the calibration from occurring, this scheme does not interfere with the rest of the device's behavior. Although delayed in this manner with the CAL input, this should still be considered the power-up calibration that must occur before proper performance can be expected.

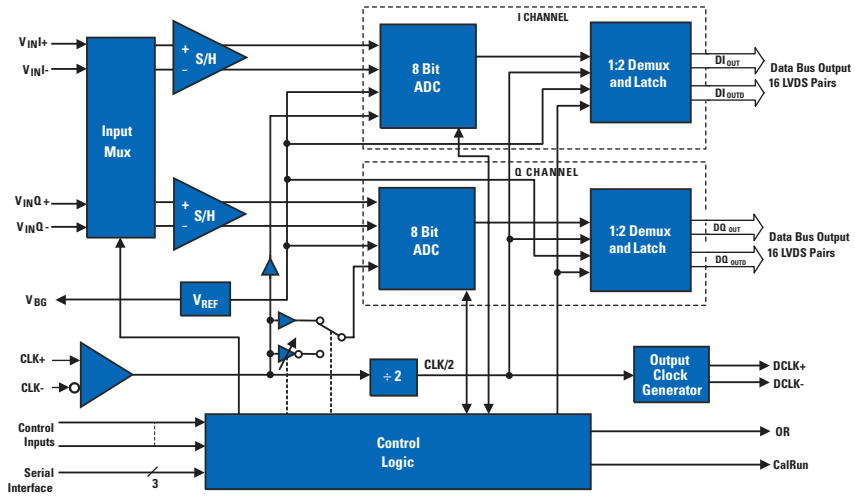

Figure 1. Block Diagram of ADC08D1500

National Semiconductor
The Sight & Sound of Information

To obtain accurate calibration, it is important for key variables to stabilize. In addition to environmental conditions (supply and temperature), the device's other operational conditions have to be stable as well.

- The clock input must be stable (this includes not performing DCLK_RST);
- The analog input is within the specified range, but the frequency is not important — including DC;
- The control/configuration settings must not be disturbed during calibration;
- The device must be in normal mode (not DES mode) for the ADC08D500/1000/1500, but not for the ADC08D1020/1520 or ADC083000/B3000;
- The control registers must not be accessed, though the SCLK may be active;
- The device should not be in power-down mode when starting calibration, nor enter power-down while calibration is underway

Device Behavior During Self-Calibration

In addition to the interruption to the signal processing path, the device has other effects during the calibration cycle:

1. The digital outputs are disabled.
2. The DCLK output is also disabled on certain devices of this family.

The DCLK output of the device is generally intended for data capture purposes only. The fact that it is interrupted means that the ASIC/FPGA device should not rely on it as a clock signal for its logic beyond the capturing logic. However, for those applications where it is essential to use the DCLK signal as a general purpose clock, the newer devices of this family give the user the control to keep the DCLK running during calibration. The cost of this is that the analog input termination resistor (Rterm) is not calibrated if the DCLK is kept active — causing the Rterm value to be slightly less accurate. Thus, this option should be used only for subsequent on-command calibration cycles.

On the devices, the Resistor Trim Disable (RTD) bit in the Extended Configuration Register controls whether the DCLK is allowed to stop ion Register controls whether the DCLK is allowed to stop during calibration or not. The default state of this bit (at power-up) is DCLK will be stopped and Rterm will be trimmed during calibration. At the time of power-up calibration, the user must leave this bit in its default state and expect the DCLK to stop during calibration. The user may clear this bit in order to keep the DCLK running during on-command calibration cycles.

Performance Effects

Guaranteed performance in the datasheet is based on the device being correctly calibrated. As with any electronic circuitry, the device exhibits some amount of performance degradation as environmental conditions change after calibration. The system parameter that usually affects performance is temperature. On-command self-calibration should be performed when temperature change exceeds a threshold. This threshold should be determined during the design process. The following observations, from limited data, may be useful to the user.

1. The ENOB performance of the device has been seen to degrade by 0.35 bits over a temperature range of 55°C (from +45°C to +100°C die temperature).

2. Gain error of 2% across an 80°C temperature range (from +20°C to +105°C die temperature) has been observed.

3. If the DCLK is enabled to run during calibration and the Rterm is not calibrated after the required power-up calibration, the Rterm value due to temperature effects alone is expected to vary by 1% from 0°C to +120°C die temperature.

A reasonable temperature variance threshold to trigger a self-calibration cycle could be in the 20 to 30°C maximum range.

Conclusion

The user is provided a great deal of flexibility to allow these devices to provide reliable performance over a wide range of temperature. By maintaining the device's temperature feedback, the sampling can be adjusted in subtle ways to allow these ADCs much better accuracy. Design solutions strive for better performance and self-calibration enables a better thermal performance. ■

For Additional Design Information

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EDITED BY FRAN GRANVILLE

pulse

INNOVATIONS & INNOVATORS

Chips improve efficiency for notebook, desktop power supplies

Digitally controlled power supplies—those in which the control loop closes digitally—have so far found favor primarily in applications requiring large amounts of power. For example, ColdWatt's (www.coldwatt.com) 1200 to 1625W ac/dc power supply uses Silicon Labs' (www.silabs.com) C8051F30x digital-power-control chip and targets server installations. Now, Marvell is introducing two digital-control chips that target smaller ac/dc power supplies for notebook and desktop computers. The 8041 aims at notebook computers and supplies as much as 80W, and the 8011 targets desktop computers and supplies as much as 300W. The chips also introduce digital PFC (power-factor correction) for these smaller supplies. Currently, EnergyStar (www.energystar.gov) standards don't require PFC for laptop and desktop supplies, but future EnergyStar revisions will include PFC requirements because of PFC's ability to increase power efficiency.

The 8041 and 8011 power-control chips can reduce supply size by as much as one-third for notebook and desktop computers.

The chips use Marvell's proprietary DSP to optimize power throughout the cycle by changing from pulse-width modulation to pulse-frequency modulation to keep the peak current at the lowest level. This architecture can also intelligently adjust the current-threshold limit for constant power to manage differences in worldwide universal voltages, which can range from 90 to 260V. Marvell claims that the chips can reduce power-supply size by one-third, reduce BOM (bill-of-materials) count by as many as 20 parts, and increase power-supply efficiency to 85%. The chips will sell for less than $2 each (1000).**—by Margery Conner**

▷**Marvell**, www.marvell.com.

FEEDBACK LOOP

"Sorry, folks, but until the laws of supply and demand actually start applying to us, you need to stop buying the chief-executive-officer spin about an engineering 'shortage.'"

—consultant David Stroup in *EDN*'s Feedback Loop, at www.edn.com/article/CA6491148. Add your comments.

802.11n WLAN comes in one chip

Broadcom has announced the BCM4322, a single-chip offering for the IEEE 802.11n Wi-Fi standard—or, strictly speaking, compliant with the 11n draft 2.0 specification, as ratification of the standard is due for 2008. With a claimed "real" throughput of more than 200 Mbps, the chip will support multimedia applications, including high-definition video streaming, according to the company. The 4322 integrates all of the functions of 802.11n, with dual radio channels for 2.4- and 5-GHz operation, power amplifiers, a MAC (media-access controller), and a baseband processor. Broadcom designed the chip in 65-nm CMOS.

The high level of integration allows, the company estimates, a reduction in BOM (bill-of-materials) costs for a WLAN subsystem of as much as 40% and a PCB (printed-circuit-board)-area reduction to approximately 150 mm^2. You can fit the WLAN function onto a PCI Express minicard format for use in laptop and other mobile computing devices.

Broadcom's main applications targets for the 4322 are home-media gateways, routers, and printers, and—considering the chip's small footprint—products that have not previously included WLAN, such as televisions, set-top boxes, and camcorders. Power is 1.6W, less than half that of Broadcom's previous chip set. Although the company acknowledges that this figure is unlikely to be in the power budget of handheld devices, it simplifies the design of a range of point-to-point WLAN products. The BCM4322 is available for sampling now, and production quantities will become available in the first quarter of 2008.

—by Graham Prophet, *EDN Europe*

▷**Broadcom**, www.broadcom.com.

PIC microcontrollers reach into 32-bit processing

Microchip's PIC32 microcontroller family brings 32-bit processing options to the PIC line of processors. Microchip based the processors on the upgraded MIPS32 M4K core, and they maintain compatibility with the company's existing line of PIC microcontrollers by supporting the same peripheral IP (intellectual-property) blocks, the same package pinouts, and the same development-tool environment. In addition to Microchip's own MPlab development tools, 11 third-party-tool vendors offer development support for the PIC32 processors with IDEs (integrated development environments), compilers, debuggers, operating systems, and software IP. According to the company, the philosophy behind the PIC32 is to maintain the essence of a PIC microcontroller but offer it with more processing performance, more memory, and more choices of development tools.

The first seven devices in the family support operation as fast as 72 MHz with as much as 512 kbytes of flash memory and as much as 32 kbytes of RAM in a 64- or 100-pin TQFP that is peripheral- and pin-compatible with Microchip's 16-bit PIC24 and dsPIC DSC (digital-signal-controller) microcontrollers. Some of the devices include as many as four channels of DMA with an integrated CRC (cyclic-redundancy-check) engine that can operate while the core is in idle mode. The family implements a single set of shadow registers of the 32-core register file. The M4K architecture that these devices employ can support as many as eight shadow sets for fast context switching, so there is room for expansion in the architecture to support fast switching for larger numbers of contexts. The hardware-vectored-interrupt controller supports as many as 63 interrupt vectors. Compatible peripherals include capture/compare/PWM timers; a 16-channel, 10-bit ADC; analog comparators; common serial interfaces; a watchdog timer, brownout, power-on-reset, and code protection; and multiple clock sources, including 8 MHz, 31 kHz, and an external source.

The PIC32 uses Microchip's two-wire or JTAG debugging interface, and the on-chip debugger supports as many as eight complex hardware breakpoints as well as nonintrusive, on-chip instruction trace. The trace module tracks the program counter, and the debugging software rebuilds much of the rest of the machine state during debugging. These devices are available now for general sampling, and the company plans production volumes for introduction during the second quarter of 2008. Prices for the PIC32 begin at $2.95 (10,000); the largest device, the PIC32MX360F512L delivers 512 kbytes of flash memory and 32 kbytes of RAM in a 100-pin TQFP for $5.30 (10,000). The devices support a −40 to +85°C temperature range.

Microchip's MPlab 8.0 adds support for the PIC32, and it works with MPlab ICD (in-circuit debugger) 2 and MPlab Real ICE (in-circuit-emulator) debugging probes. The MPlab C32 C compiler uses the same peripheral libraries as the 16-bit PIC devices. The PIC32 DM320001 starter kit is available now for $49, and it includes sample code and projects, tutorials, and TCP/IP (Transmission Control Protocol/Internet Protocol) and FAT (file-allocation-table)-16 stacks. Microchip's software libraries include source code for boot loader over IP, FTP (file-transfer-protocol) server, SMTP (Simple Mail Transfer Protocol) agent, and a Web server. Expansion boards supporting Ethernet, a QVGA-touchscreen display, and an I/O daughterboard will be available for the starter kit in the fourth quarter of this year.

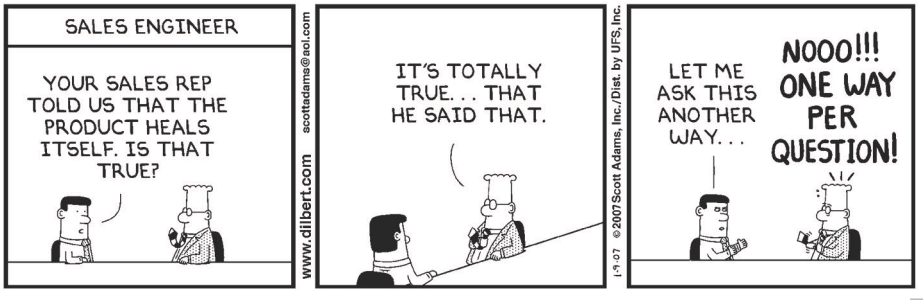
—by Robert Cravotta

▷**Microchip**, www.microchip.com.

The PIC32 adds 32-bit microcontrollers to the PIC family of 8- and 16-bit processors.

This starter kit is now available to get you started working with the PIC32 family.

DILBERT By Scott Adams



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Transceiver features multiband digital downconverter

Currently available communications protocols and new requirements for wireless-Web digital services have produced numerous wireless standards, each with unique signal requirements. To address these new standards, Pentek recently released the Model 7142-428 digital transceiver with a multiband DDC (digital downconverter) and an interpolation filter. The transceiver is a complete software-radio system in an off-the-shelf PMC/XMC form factor. The module employs four ADCs and one DAC that can operate at bandwidths exceeding 40 MHz for direct connection to the HF or IF ports of communications or radar systems.

By offering a range of more than four orders of magnitude for both decimation and interpolation, the Model 7142-428 addresses a wide range of commercial and military communication systems. In a transceiver, the decimation factor

The Model 7142-428 PMC/XMC from Pentek is a complete software-radio system with input and output signal bandwidths of 8 kHz to 40 MHz.

and interpolation factor determine the ratio between the IF frequency and the bandwidth of the received and transmitted signals. Pentek implements the 428 IP (intellectual-property) core as two cascaded DDC stages, each with a programmable decimation of one to 256. Because the decimations from the two stages multiply, users can choose an overall decimation of two to 65,536. Four 14-bit ADCs at the front end operate at sample rates as high as 125 MHz. Each of the four identical DDC engines uses an independent four-input multiplexer to select any one of these four ADCs as its input source. The four DDCs feature independent tuning and decimation to translate any frequency band at the input down to zero frequency.

On the upconverting side, a Texas Instruments (www.ti.com) DAC5686 offers a 500-MHz, 16-bit DAC and a DUC (digital upconverter) operating at a sample rate as high as 320 MHz. The DUC has a built-in interpolation range of only two to 16; however, the 428's IP core-interpolation filter extends this range by an additional factor of two to 2048, providing an overall range of two to 32,768. This extended DUC-interpolation range matches

> The Model 7142-428 addresses a wide range of commercial and military communication systems.

the DDC-decimation capabilities of two to 65,536, offering symmetrical support for transmitting and receiving functions for signals of any bandwidth. After interpolation, you can tune the DUC to translate the baseband-transmitting-signal frequency to any IF output frequency as high as 140 MHz. Pentek supports all of the 428 IP core functions with a board-support package and software-development tools compatible with the Windows, Linux, and VxWorks operating systems. The Model 7142-428 PMC/XMC sells for $15,500, and delivery is eight to10 weeks.

—by Warren Webb

▷**Pentek Inc**, www.pentek.com.

FPGA-design environment squeezes power consumption

EDA tools for FPGAs and ASICs commonly include optimization capabilities for timing and gate efficiency, but Actel claims that its new Libero Version 8.1 package is the first FPGA development tool to include low-power-optimization capability. The company has been promoting the miserly static- and dynamic-power consumption of its flash-based FPGAs, and the software tool allows designers to achieve additional power savings.

Company Chief Executive Officer John East points out that not only mobile products, such as cell phones, but also medical and industrial products run on battery power and demand low power consumption.

Libero 8.1 attacks power consumption in four ways. First, the tool offers the aforementioned power-optimized-layout option, which the company claims can cut dynamic-power consumption by 30%. Second, the tool allows designers to analyze power profiles, such as active and sleep modes, and estimate battery requirements. Third, the tool can run an analysis on an FPGA layout and provide power-draw requirements for portions of the design, such as clock domains. Moreover, the tool can perform a cycle-accurate power analysis. Finally, a switching-analysis option can identify hazards or spurious signal transitions that waste power.

Actel offers a Platinum edition of Libero 8.1 for $2495 for Windows or Linux. A more feature-limited Gold edition is free for Windows. The company also has just announced what it claims are the smallest FPGAs on the market. The newest Igloo family members measure 4×4 mm. Prices for the 30-000-gate AGL030 start at $1.50 (volume quantities).

—by Maury Wright

▷**Actel**, www.actel.com.

FEEDBACK LOOP

"Myths proliferate in the low-level technical world."

—reader Hector Ibarra, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6418215, where columnist Howard Johnson addresses some of those myths. Add your comments.

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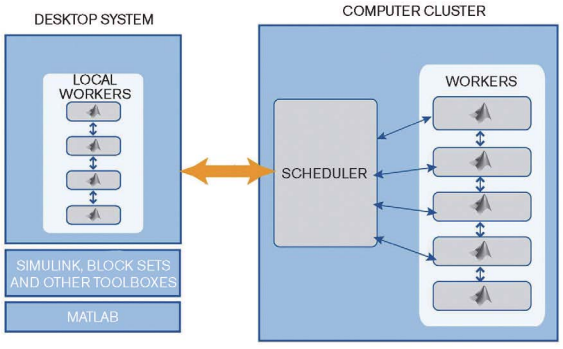
Matlab adds support for parallel applications, multithreaded computations, 64-bit platforms

To help engineers and scientists model increasingly complex systems in less time by allowing development of parallel applications independently of the resources that are available for execution, The MathWorks recently announced four enhancements in its Matlab and Distributed Computing Toolbox products. The enhancements allow increased performance and large-data-set handling.

Matlab now supports multithreaded computation for multicore systems and 64-bit Solaris platforms. Distributed Computing Toolbox now offers designers the ability to develop applications that interleave parallel and serial code and interactively prototype parallel algorithms on a desktop computer by running four local Matlab sessions. With Matlab and Distributed Computing Toolbox, engineers can prototype parallel applications on multicore desktop computers using as many as four processors and four Matlab sessions. For more computing power, these applications can scale to a computer cluster without code change by using the Matlab Distributed Computing Engine. The applications can also include serial code that executes in the desktop machine.



The Distributed Computing Toolbox enables application prototyping on a desktop with as many as four local workers (left), and, with the Matlab Distributed Computing Engine (right), you can scale applications to multiple computers on a cluster.

Using the multithreading feature, Matlab applications using elementwise and linear-algebra functions can leverage multicore machines by simultaneously running multiple threads for improved performance. The 64-bit Solaris support allows engineers using Matlab to exploit the benefits of 64-bit computing to develop applications involving large data sets and computationally intensive tasks. Matlab 7.5 is available now for the Microsoft Windows, Solaris, Linux, and Macintosh platforms. US list prices start at $1900.

US list prices for the Distributed Computing Toolbox 3.2 start at $1000. Prices for the Matlab Distributed Computing Engine start at $6000.

—by Ann Steffora Mutschler

▷**The MathWorks**, www.mathworks.com.

DaVinci processor targets HD transcoding

Texas Instruments' DaVinci DSP-based TMS320DM6467 system includes targeted video accelerators that deliver multiformat HD (high-definition) transcoding in a single device. The programmable system centers on the C64x+ DSP core running at 600 MHz and the ARM926EJ-S core operating at 300 MHz. These speeds match those of previous DaVinci devices because the as-much-as-tenfold processing-performance improvement comes mainly from the integrated hardware accelerators; less than 300 MHz of the DSP's processing performance is necessary for managing and performing multiformat transcoding. The DSP core includes 32-kbyte L1 instruction and data caches, a 64-kbyte boot ROM, and a 128-kbyte L2 cache. The ARM core includes an 8-kbyte data cache, a 16-kbyte instruction cache, an 8-kbyte boot ROM, and 32 kbytes of tightly coupled memory.

The HD-targeted hardware accelerators differ from the DM6446 system by stripping out circuitry that provided flexibility and optional functions to focus only on those functions that will deliver the highest transcoding-processing efficiency. The encoding/decoding software available with the device takes advantage of the restructured hardware accelerators in the HD-VICP (high-definition-video/imaging coprocessors). The HD-VICP supports 1080p at 30 frames/sec, 1080i and 720p at 60 frames/sec, or even simultaneous SD (standard-definition) H.264 BP at 30-frame/sec encoding and decoding. The algorithms available support H.264 HP (high-profile), MPEG-4, VC (video codec) 1, and MPEG-2 encoding and decoding. The video-data-conversion engine has likewise undergone an optimization for HD transcoding and provides support for chroma sampling instead of a previewer, downscaling instead of a resizer, and menu overlays. The system includes video ports for two 8-bit BT.656 or one 16-bit BT 1120 for capture and display.

The DM6467 is available for sampling for $35.95 (50,000). The DVEVM (DaVinci evaluation module) for the DM6467 processor will be available during the first quarter of 2008 for $1995. The development environment builds on MontaVista Linux LSP (Linux-support package), open-source Linux, and DaVinci APIs (application-programming interfaces). The multimedia codecs include the aforementioned video formats, as well as AAC (advanced audio coding), AC (audio compression) 3, and MP3 audio encoding and decoding; G.711 and G.723 speech encoding and decoding; JPEG encoding and decoding; and new support for transcoding between MPEG-2 and H.264.

—by Robert Cravotta

▷**Texas Instruments**, www.ti.com.

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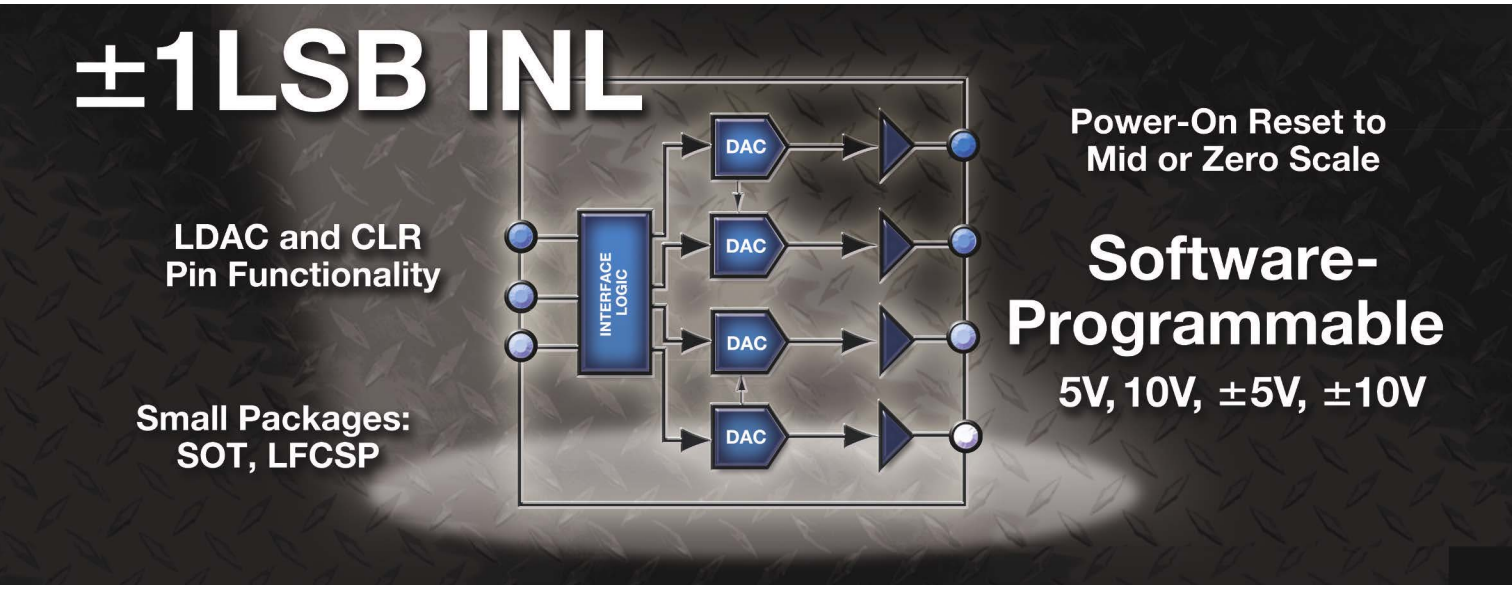

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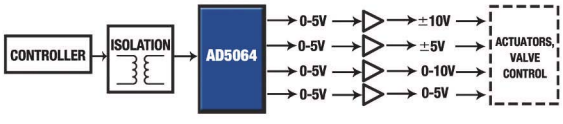

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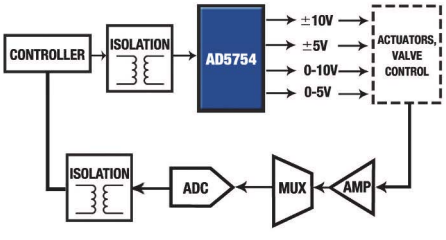

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ANALOG DEVICES

RESEARCH UPDATE

BY FRAN GRANVILLE

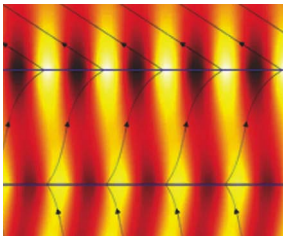
Taming tiny, unruly waves for nanoscale optics

Researchers at the Georgia Institute of Technology have discovered a way to predict the behavior of unruly waves of light during nanoscale radiation-heat transfer, opening the door to the design of a spectrum of new nanodevices and nanotechnologies, including solar thermal-energy technologies. Lead researcher Zhuomin Zhang and his team set out to study evanescent waves in nanoscale-radiation-energy transfer between two very-close surfaces at different temperatures by means of thermal radiation. Because the direction of evanescent waves is seemingly unknowable (an imaginary value) in physics, Zhang's group instead decided to follow the direction of the electromagnetic-energy flow, or Poynting vector, rather than the direction of the photons, to predict behavior.

The Georgia Tech team observed that, instead of normal straight-line radiation, protons tunneled through the vacuum between two surfaces just nanometers apart. The team also noticed that the evanescent waves were separating during this thermal process, allowing the scientists to visualize and predict the energy path of the waves.

Understanding the behavior of such waves is critical to the design of many devices that use nanotechnology, including near-field thermophotovoltaic systems, nanoscale imaging based on thermal-radiation-scanning-tunneling microscopy, and scanning-photon-tunneling microscopy. For more, go to www.me.gatech.edu/~zzhang.

▷**Georgia Institute of Technology**, www.gatech.edu.



Waves of electromagnetic energy pass through a vacuum between two plates of silicon carbide just 100 nm apart—one at an elevated temperature. The lines represent the energy stream bending the light as it pushes through the small gap.

Smart optical microchips could advance telecom

Researchers at the Massachusetts Institute of Technology have developed a theory that could lead to "smart" optical microchips that adapt to different wavelengths of light, potentially advancing telecommunications, spectroscopy, and remote-sensing technologies.

In the macroscopic world, light waves do not exert significant forces. In the microscopic world, however, photons bouncing off the walls of a cavity couple with ultrapure laser light to build up a measurable force—radiation pressure—similar to the pressure that gas molecules in an aerosol can exert. To take advantage of this pressure, the researchers propose machines built from ring-shaped cavities only millionths of a meter in size located on the chip surface. Pressure on the cavity walls gets high enough to force the cavity to move. This movement forms a critical part of an optical micromachine, which adjusts its configuration to respond to light in a predesigned way.

Using the concept, a "smart" resonator could chase the frequency of the laser light incident upon it. As the frequency of the laser beam changes, the frequency of the resonator always follows it. In other words, this new resonator is like a wineglass that self-adjusts to the pitch of a singer's voice and follows it along through a song. Coupling the resonating cavities with nanoscale cantilevers allows the creation of optical devices analogous to MEMS (microelectromechanical-system) devices.

▷**Massachusetts Institute of Technology**, www.mit.edu.

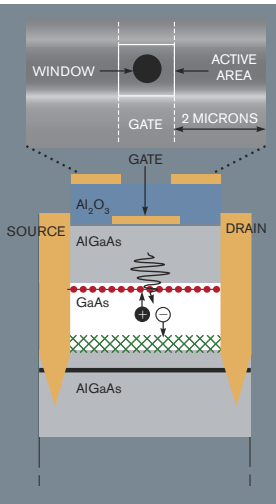
QUANTUM-DOT TRANSISTOR COUNTS INDIVIDUAL PHOTONS

The NIST (National Institute of Standards and Technology) has designed and demonstrated a FET containing quantum dots that can count individual photons—the smallest particles of light. Designers could easily integrate the semiconductor device into electronics, and it may be able to operate at higher temperatures than other single-photon detectors—practical advantages for applications such as quantum-key distribution for "unbreakable" encryption using single photons.

The NIST device can accurately count one, two, or three photons at least 83% of the time in response to any small number of photons. The device contains approximately 1000 quantum dots, nanoscale clusters of semiconductors with unusual properties. NIST custom-designs the dots to have the lowest energy of any component in the detector. Applying a voltage to the detector produces an internal current, or channel.

The device currently detects single photons at wavelengths of approximately 800 nm. By using different semiconductor materials, NIST researchers hope to make detectors that respond to the longer, near-infrared wavelengths that telecom uses.

▶National Institute of Standards and Technology, www.nist.gov.



NIST's modified FET can count single photons, or particles of light. When light enters through the transmission window (top), it penetrates the gallium-arsenide absorbing layer and separates electrons from the "holes" they formerly occupied. Quantum dots (red) trap the positively charged holes, while electrons flow into the channel (green). By measuring the channel current, research can determine the number of absorbed photons (courtesy NIST).

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ANALOG DEVICES

BY HOWARD JOHNSON, PhD

Lossless propagation

Inject a fast rising edge into a long, uniform transmission structure. Imagine the signal propagating with uniform velocity and negligible attenuation for some distance.

Figure 1 depicts two snapshots taken at times t_1 and t_2. Each snapshot shows the voltages on the transmission line at that moment. At time t_1, the midpoint of the rising edge has just reached point x_1. At time t_2, it reaches the further point, x_2.

I drew an L-C ladder model to represent the transmission line. The model incorporates both parasitic capacitance and inductance. As long as the rising edge spans several sections of the model, and it does in this example, the L-C model accurately represents the behavior of a typical PCB (printed-circuit-board) transmission line from a digital application.

Look at the difference between the voltage waveforms at times t_1 and t_2. As the rising wavefront moves between points x_1 and x_2, it charges the parasitic capacitors in the diagram from a ground state (no voltage) to a voltage of V_{CC}.

Between times t_1 and t_2, enough electrical charge must enter the circuit to change the voltage on those capacitors from ground to V_{CC}. In this example, the charge emanates from the driver. It's the only source of power in the circuit.

If you believe in lossless propagation—that is, if you believe the rising edge propagates without sensible degradation, at a constant velocity, without significant loss of amplitude—then you must also recognize that in each similar unit of time, the rising-edge waveform charges a uniform amount of capacitance. In other words, during every unit of time, the circuit requires a uniform deposit of charge. A steady flow of charge into the circuit means that the driver must supply a constant current.

This simple argument ties together a number of important facts—namely, that uniform propagation of a constant step edge *requires* a constant flow of current from the driver.

Therefore, in the short term, *the input impedance of a uniform, lossless, distortionless transmission line appears purely resistive*. No other circuit but a resistor demands a constant current in response to a step change in voltage. If the circuit requires a uniform current, it looks like a resistor.

The properties of lossless propagation and resistive input impedance are inextricably linked. You can't make a lossless-propagation medium without it also having a purely resistive input impedance (in the short term).

Now, after your rising-edge signal strikes the endpoint, reflects, and returns to the source, something different happens. Propagation no longer remains uniform in that case. The input impedance of the structure may no longer appear purely resistive. That's a different story.

For any short-term event—anything to do with rise time, crosstalk, ground bounce, or other signals so short that they haven't time to get to the end of the line and return before the whole event is over—the input impedance of a PCB transmission line appears purely resistive. EDN

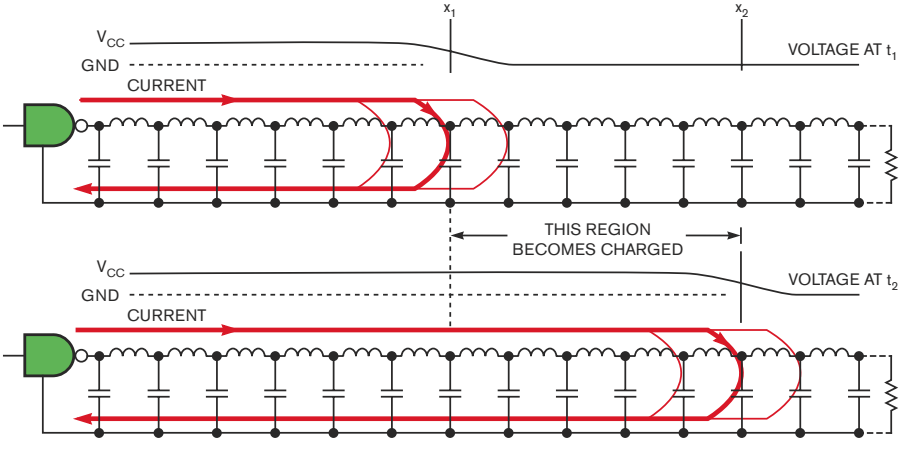
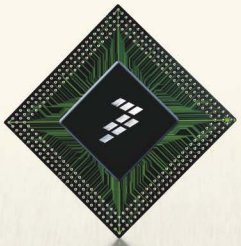


Figure 1 A steady stream of current from the driver propagates a lossless step edge.

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.



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BY PALLAB CHATTERJEE, CONTRIBUTING TECHNICAL EDITOR

Grid and resolution

A recent trend confusing two quite different terms has had a huge negative impact on the yield, reliability, and manufacturability of DSM (deep-submicron) and subwavelength semiconductor designs. This trend is the confusion and interchange of the terms "grid" and "resolution" with respect to the physical-design database.

Resolution refers to the minimum database unit that the physical-design database stores. For a standard GDSII (Graphic Design System II) stream file, the resolution is 0.001 micron for metric designs. In contrast, grid refers to the minimum pitch of the grid where the layout designer aligns objects during placement. The grid is an integer multiple of the resolution. Additionally, the grid size is proportional to the minimum electron-beam-spot size used to create the masks for the design. On a typical 130- or 90-nm design, the grid is typically 0.01 micron—10 times the resolution.

Most process-design-rule documents specify the working grid to ensure compatibility with the mask-generation processing. The inherent database resolution is usually unspecified and assumed for the GDSII or OASIS (Open Artwork System Interchange Standard) database. The assumption of the manufacturing-process flow is that the data appears with all edges and vertices on the design grid. As a result, the information transfers to the MDP (mask-data-prep) stages with all the design information intact.

Historically, layout engineers and those familiar with the full set of design rules would set up most layout tools. But today, software developers lacking a complete understanding of the engineering requirements of the grid parameter are the ones who develop many of the technology files that vendors distribute as downloadable infrastructure. As a result, most of the custom-layout and IP (intellectual-property)-placement design-technology files have the grid parameter set equal to the resolution parameter at 0.001 micron. Redrawing and zooming time increases because of the fine resolution and the large number of objects you are assembling. This increase immediately impacts the parameter setting, reducing design throughput.

Most of the custom-layout and IP-placement design-technology files have the grid parameter set equal to the resolution parameter.

A more disastrous result is the failure of the DRC (design-rules checking) that occurs when edges are not on the grid. The verification and MDP routines snap the design data to the planned grid and either increase or decrease the width or the spacing of layout objects. This adjustment can result in a change of the IC design's function and operation.

Many of the new DFM (design-for-manufacturing) tools implementing RET/OPC (resolution-enhancement-technology/optical-proximity-correction) applications also assume that the grid parameter relates to the mask-making process and differs from the resolution of the database. For example, DFM tools increase spacing on the layout by moving edges and vertices of the design. If the data is not on the grid—for example, the grid is a multiple of 0.01 micron but an object is at 0.014 micron—then spacing changes may not result in a fix to properly resolve a spacing issue. Additionally, when you add new corner serifs or artifacts to a design, they are on the masking grid. When designs are not on this same grid, the new OPC objects either do not extend to their full distance from the existing structures or have a gap between the OPC object and the design object. As a result, this scenario severely reduces the OPC's improvement on off-grid data.

For the assembly and final release of DSM and subwavelength designs, it is essential to clean up IP, making it compatible with the mask-making grid before the MDP and RET phase of the design. The verification of the IP, custom blocks, and Pcells must be complete for the grid compliance on the actual mask-transfer database, not just the working data of a design. EDN

Contact me at pallabc@siliconmap.net.

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BY JOSHUA ISRAELSOHN, CONTRIBUTING TECHNICAL EDITOR

Protect yourself

This installment of "Analog Domain" focuses on one of the growing circuit-implementation challenges that confronts IC, subsystem, and system designers alike: interface ESD protection. Two trends make interface protection increasingly difficult as we move along our industry's current technology trajectory. First, increasing demands for processing speed and functional density have pushed IC fabricators to shrink further the minimum dimensions of MOS devices. For a given gate dielectric, device physics require maintaining the dielectric thickness in proportion to lateral dimensions (**Reference 1**). Thinner dielectrics, however, are more susceptible to ESD overstress.

Second, port speeds continue to increase, particularly with the growing success of portable-media devices. As one example, the 1996 USB 1.0 release provided for 12-Mbps interfaces. Four years later, a USB 2.0 feed could reach 480 Mbps. The yet-unreleased USB 3.0, shown at this year's Intel Developer Forum, trades copper interconnect for parallel fiber-optic cable to attain a 4.8-Gbps connection. IEEE 802.3 (Ethernet) and IEEE 1394 (Firewire) show the trend to a greater or lesser degree.

Traditionally, ICs include ESD-shunting structures within their standard interconnect-pad cells, which protect the internal circuitry from ESD strikes to the device's pins. The on-chip-ESD protection may be all that's necessary to see an IC safely from its manufacturer to a board assembler if both organizations adhere to strict anti-ESD-handling procedures. Though on-chip-ESD structures serve as excellent *secondary* protection, however, they are usually insufficient to protect an interface over years of exposure in uncontrolled environments.

The reasons these structures are insufficient are twofold: They are too small to absorb large energy transients that interfaces commonly experience in the field, and they reside too far away from the interface-entry point to prevent coupling to adjacent traces. Once an I/O line's on-chip-ESD cell begins to conduct, a current transient develops along its trace, exciting the trace's inductance, causing a corresponding voltage transient, Ldi/dt. Adjacent conductors with mutual inductance to the I/O trace see coupled transients that can exceed the capabilities on their own on-chip-ESD cells. These adjacent traces can include clock, data, or other nonported signals (**Reference 2**).

Mounting TVSs (transient-voltage suppressors) as close to the entry point as possible alleviates this problem by shunting the ESD event to ground before transient currents develop inside your product. Doing so can add substantially to your product's robustness with minimal additional cost. "If a finger can get close to a node, protect it," is a good rule of … errrrr … thumb. This rule applies to keypad switch lines, too, despite their insulating keycaps.

High-speed interfaces require TVSs with particularly low shunt capacitances. Check your vendor's product line for devices built for specific high-speed interfaces. If you don't find devices specifically for your interface, compare your signaling frequencies and source-and-line characteristics with those of interface standards that the vendor explicitly supports. When considering TVS manufacturers' claims, be sure to understand which ESD source model they use when specifying their devices. The JEDEC HBM (human-body model), for example, uses a 100-pF capacitor discharging through a 1.5-kΩ resistor. The repeatability of the test method's results has been historically an area of concern (**Reference 3**). The IEC-61000-4-2 standard's test method promotes repeatability, and its source model—150-pF behind 150Ω—is more demanding of your design. EDN

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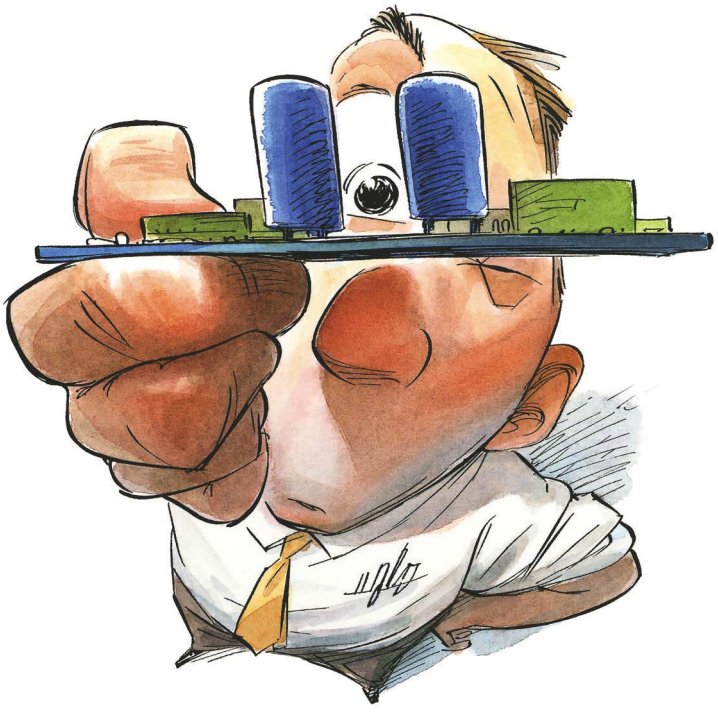

I recently had to revamp one of my company's more-than-30-year-old designs. Like any project these days, the new design needed to be smaller, cheaper, include many more functions, and see completion in a relatively short time. To decrease risk, I chose to reuse much of the physical interface from the previous design, including a transformer-isolated interface to the outside world. However, the constraints of a smaller design, coupled with the new functions I was adding, did not allow for 100% reuse of the existing components for this interface.

Scratching for PCB (printed-circuit-board) space, I decided to modify the six transformers that provided the isolation to the outside world from a square-shaped, double-E-core design to a more volumetric-efficient, circular pot-core design. The company developed the previous design when design documentation was not mandatory, so I did not have a set of requirements on which to base the new transformer. However, as long as I kept the turns ratio the same, the wire gauge appropriate, and the flux density similar, I thought the risk should be low. I exactly followed this method and also ran a worst-case calculation to verify plenty of margin due to saturation. I used the voltage-based flux-density equation for transformer saturation ($B=[V\times10^8]/[4\times N\times A_C\times f]$), where B is flux density, V is applied voltage, N is the number of turns, A_C is the cross-sectional area, and f is the applied frequency. It turns out that my design had more than 50% saturation margin.

To further reduce risk, we ordered several prototypes from an overseas vendor that our supply chain recommended because of its low overall cost. Due to low volumes of the prototype run, a US factory rather than the regular overseas production facility produced the samples. The prototypes performed flawlessly, and we released the new design on time, under budget, and within scope.

A few months after fielding several units, we received a report that the new design was failing intermittently in the field. After visiting the field several times and running multiple tests in the lab, we attributed the failures to interactions with another piece of equipment at the outside-world interface. The puzzling thing was that we had tested compatibility with this equipment many times before release. Even more frustrating was that it appeared that the root cause was saturation of the new transformer design! How could this be? We had plenty of design margin and tested multiple samples. We found the old modules with the sample transformers with which we had initially qualified the design. When we applied this hardware to our test setup, we could not reproduce the failure. Using the hardware from the field, however, the failure was reproducible. Now we had to determine the difference between the two versions of hardware.

The new transformer design used an ungapped pot core that was less costly and easier to obtain than a gapped pot core. And it appeared to meet the saturation requirements with plenty of margin. However, we did not consider transient saturation due to current rather than voltage in our design calculations. It turns out that, in the prototype samples we tested, the two pot-core halves were not completely pressed together, thus creating an unwanted air gap. Because the pot core was dipped in polyurethane, the unwanted gap was permanently fixed. This unintended air gap was enough to keep the sample transformers from saturating. Once we moved production of the transformers to the overseas factory, that facility correctly built the transformers without an air gap. These transformers saturated in the field, and we had to change the modules. The good news was we didn't have many units in the field. EDN

Jeff Fries is a principal systems engineer with GE Transportation. Like Jeff, you can share your tale and receive $200. Contact Maury Wright at mgwright@edn.com.

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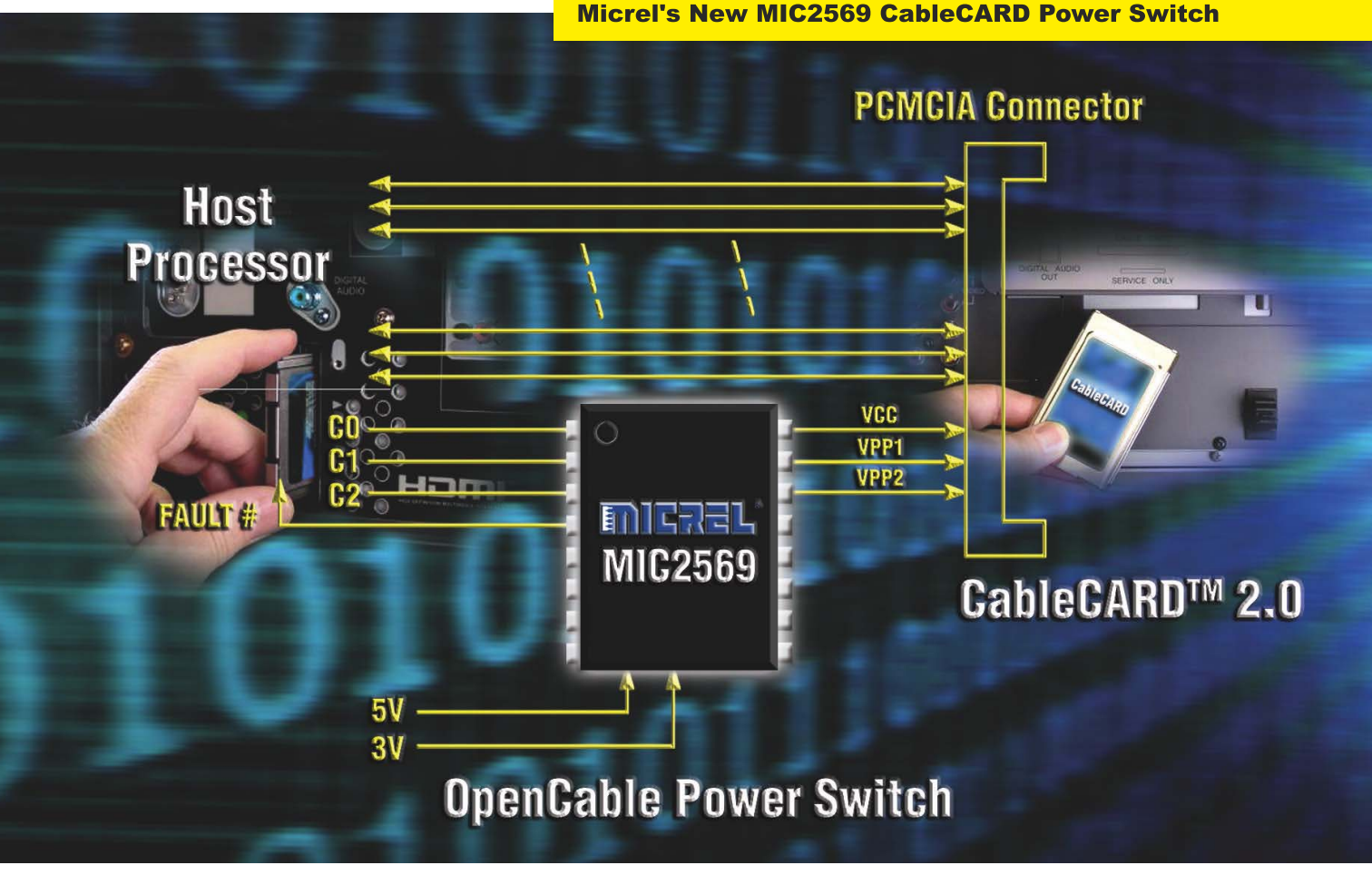

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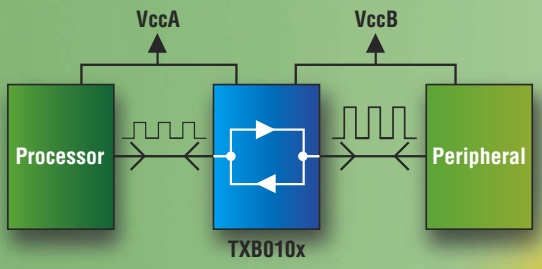
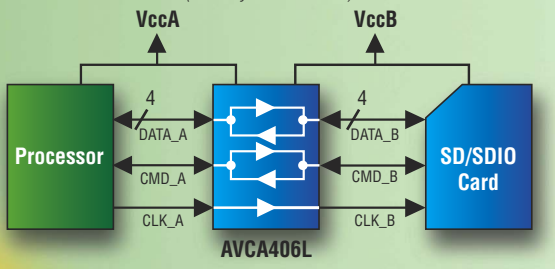
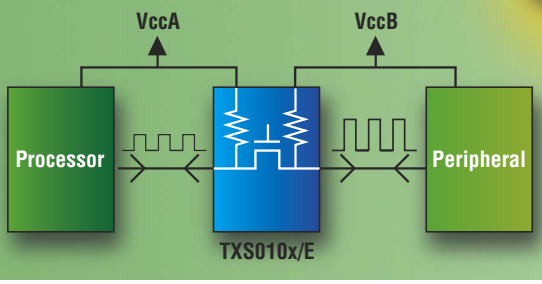


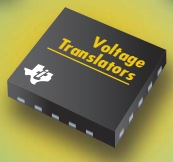
Application-Specific Translators

(Memory Card Interface)

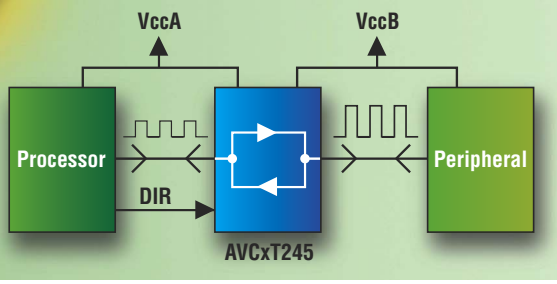


Auto-Direction-Sensing Translators for Open-Drain Applications





Dual-Supply-Configurable Translators



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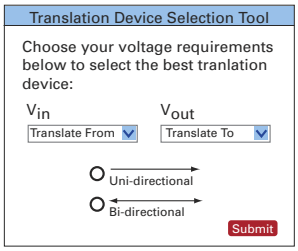
TXS0104E	4	1.65 to 3.6	2.3 to 5.5	10-kV Air Gap Discharge (IEC)	12-ball BGA
TXB0104	4	1.2 to 3.6	1.65 to 5.5	15-kV HBM	12-ball BGA
TXB0108	8	1.2 to 3.6	1.65 to 5.5	15-kV HBM	20-ball BGA
Application-Specific Translators (Memory Card Interface)					
AVCA406		1.4 to 3.6	1.4 to 3.6	15-kV Air Gap Discharge (IEC)	48-ball VFBGA
AVCA406L		1.2 to 3.6	1.2 to 3.6	6-kV HBM	20-ball VFBGA
CF4320H		1.65 to 3.3	3.3 to 5	15-kV HBM	114-ball LFBGA
Dual-Supply Configurable Translators*†					
SN74AVC1T45	1	1.2 to 3.6	1.2 to 3.6	2-kV HBM	6-bump WCSP
SN74AVC2T45	2	1.2 to 3.6	1.2 to 3.6	8-kV HBM	8-bump WCSP
SN74AVC8T245	8	1.2 to 3.6	1.2 to 3.6	8-kV HBM	24-pin QFN
SN74AVC16T245	16	1.2 to 3.6	1.2 to 3.6	8-kV HBM	56-ball VFBGA
SN74AVC32T245	32	1.2 to 3.6	1.2 to 3.6	8-kV HBM	96-ball LFBGA

** Other bit-width options available. † Bus Hold feature available.*



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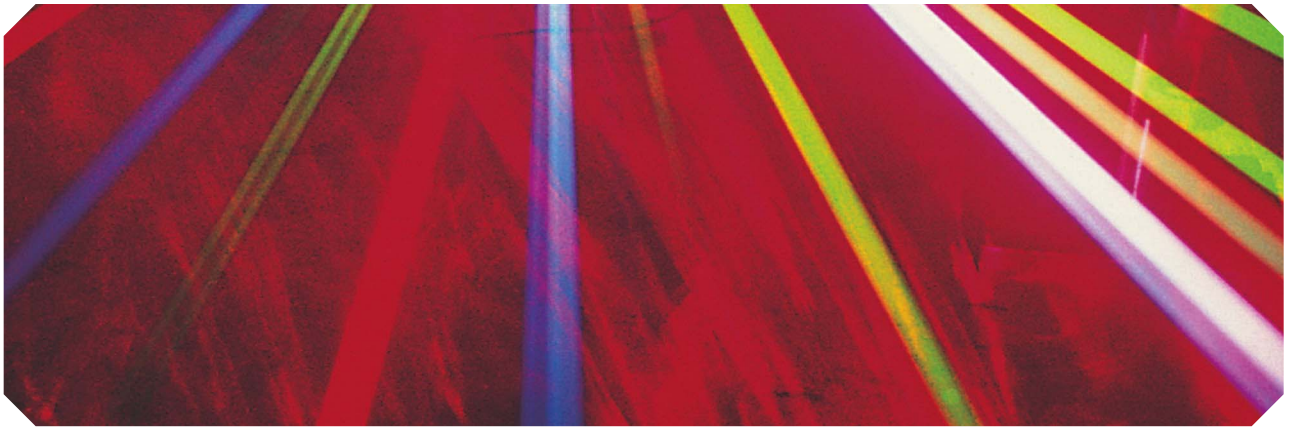


WITH A NEW MULTIPLE-STROBE TECHNIQUE, YOUR ATE CAN FIND THE PASSING SETUP-AND-HOLD MARGINS DURING HIGH-VOLUME PRODUCTION TESTING OF SOURCE-SYNCHRONOUS CIRCUITS.

PHASE STEPS
OVERCOME SLIM TESTING MARGINS

BY STEFAN WALTHER AND GUIDO SCHULZE • VERIGY

With many circuits and systems using clocks faster than 1 GHz, common-phase jitter, drift, and clock skew can affect measurements such as setup-and-hold times. ATE (automated test equipment) typically strobes clock and data signals using a single strobe with fixed timing that cannot accommodate dynamic phase shifting. To remedy this inadequacy, you can employ a technique that applies a series of strobes—each slightly shifted in phase relative to clocks and data—to accurately test and characterize signals in I/O interfaces, such as DDR SDRAM.

As signal propagation along on-chip interconnects became a limiting factor in device speeds, circuit designers turned to source-synchronous interfaces to alleviate long clock runs. Source-synchronous interfaces receive a master clock and create a local clock for nearby circuits. Local clocks reduce problems that are the fault of power-supply peaks, power and ground noise, local thermal heating, and EMI (electromagnetic interference).

Shifts in a signal's phase can change the circuit timing relative to the ATE, a factor you must keep in mind when testing a source-synchronous interface above 1 Gbps. (See **sidebar** "Source-synchronous interfaces" for an explanation of how the interfaces work.)

Static skew between a local clock and the system clock isn't difficult to overcome. You can use an output-dependent-timing test method to measure setup-and-hold times. With this approach, the test system determines the phase of the transitions in the clock and in the data signals and then sweeps a compare strobe across the timing signals while it monitors the error count. The tester then assigns the correct compare-strobe timing, which it keeps for the remaining device tests. The phase of the transitions should be stable from bit to bit and shouldn't contain excessive drift or jitter.

Figure 1 shows that, for conditions of skew only, the phase of transitions between a reference clock and a source-synchronous circuit's clock remains constant. Thus, an ATE system, which provides the reference clock to the DUT (device under test) during testing, can measure setup-and-hold times with a fixed strobe that has constant phase relative to the output clock and data.

At clock speeds greater than 1 Gbps, drift and jitter can prevent the phase of both the clock and data from remaining constant during the transmission of a data pattern. Thus, the output clock and data

THIS ARTICLE ORIGINALLY APPEARED IN THE OCTOBER 2007 ISSUE OF *TEST & MEASUREMENT WORLD* (WWW.TMWORLD.COM/ARTICLE/CA6482914).

lines of a source-synchronous interface reduce the timing margin associated with a fixed-phase strobe (**Figure 2**). Because the data and clock are synchronized, the phase variations represent a common-phase jitter that doesn't affect the data transmission.

But common-phase drift and jitter do affect measurements if you use a fixed-phase strobe, because, when the amplitude of the common-phase jitter is large enough, the moving transitions consume the entire margin, causing failures as soon as the transitions cross the fixed strobe positions. The common-phase drift and jitter cause a data eye to close more than in the device's real application. Therefore, you can't determine parametric (setup- or hold-time) data related to the dynamically changing phase of the source-synchronous clock.

Figure 3 highlights the impact of the common-phase jitter. To illustrate the problem, the bits are rotated counterclockwise by 90° so you can see how the phase of the transition points changes over time. The data's transition points and clock edges track the sine wave that represents jitter amplitude and shape. When the jitter is minimal, the transition points and clock edges still align with the ATE system's fixed-phase strobe (left-pointing arrows), but timing violations occur in some bits (lightning bolts) because of drift and jitter.

To address the timing problem, a software-based method tests source-synchronous interfaces even when the common phase shows dynamic variations in drift and jitter. The method uses traditional "capture-and-compare"-pin electronics. It scales with the available hardware, and you can easily adapt it for your application.

This method uses multiple strobes that scan bit cycles to determine where clocks and data will produce accurate measurements of setup-and-hold time. By scanning the cycles with multiple strobes, you can identify whether at least one strobe setting fulfills the setup-time specification of the DUT. Strobe settings in each cycle that don't show errors for the clock or for the data confirm a valid setup. These error-free strobe settings occur at different phases for each bit cycle N (**Figure 4**). If at least one phase-scan step in the cycle passes, then a cycle fulfills the setup-time specification.

In **Figure 4**, the cycle N–1 yields a pass for strobe settings 2 through 5 on the data-bit line and for strobe settings 1 through 3 on the clock line. Phase steps 2 and 3, in which both data and clock lines pass, represent valid test setups. The error-free phase margin for cycle N–1 is one phase step.

AT A GLANCE

- Shifts in a signal's phase can change the circuit timing relative to the ATE (automated test equipment) when you test a source-synchronous interface operating faster than 1 Gbps.
- A software-based, capture-and-compare method addresses the timing problem for testing source-synchronous interfaces.
- Because test time translates into cost, you must determine a reasonable trade-off for the test coverage.
- The test method lets you perform both measurement and validation of timing parameters with fast throughput.

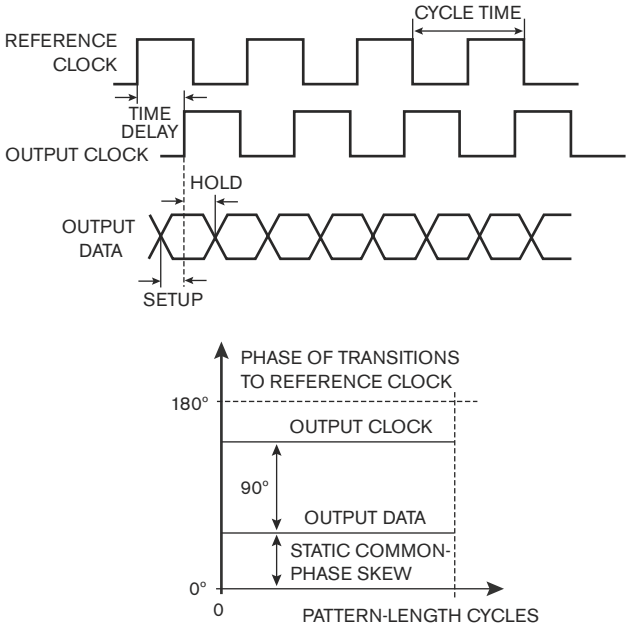


Figure 1 In the presence of only static skew to the reference clock, the phase of output-clock and -data transitions is stable over time.

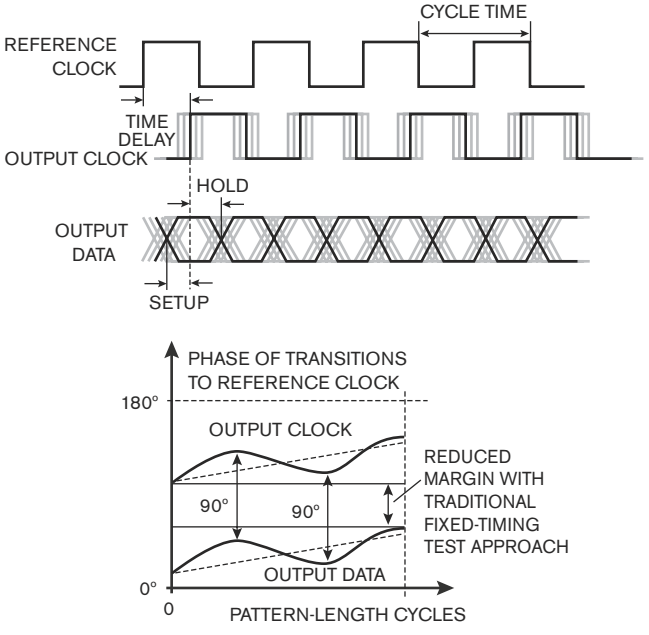
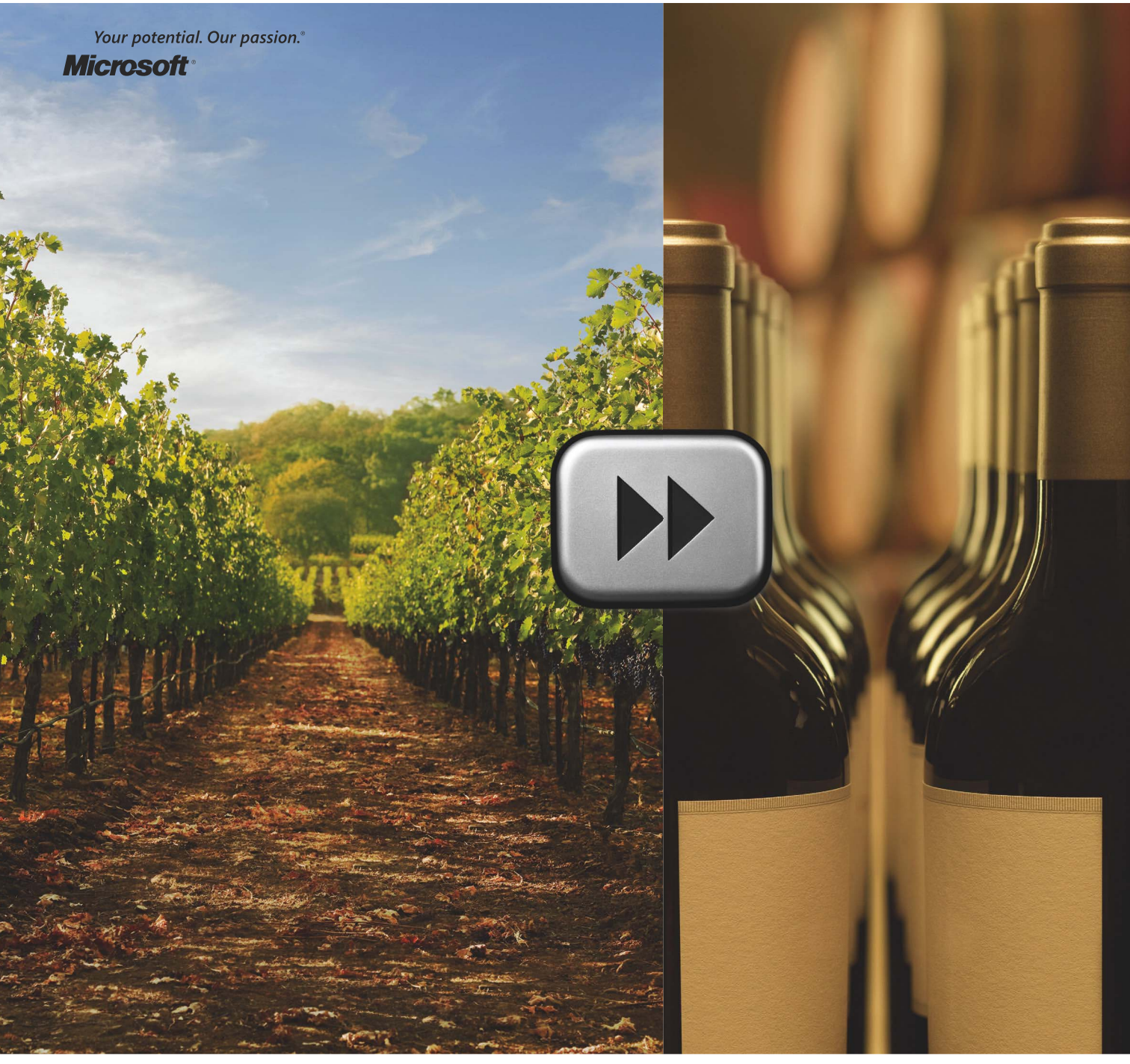


Figure 2 In the presence of dynamic common-phase drift and jitter, the phase of output-clock and -data transitions with respect to the reference clock changes over time, reducing the chance of accurate measurements of setup-and-hold time with a fixed ATE strobing point.



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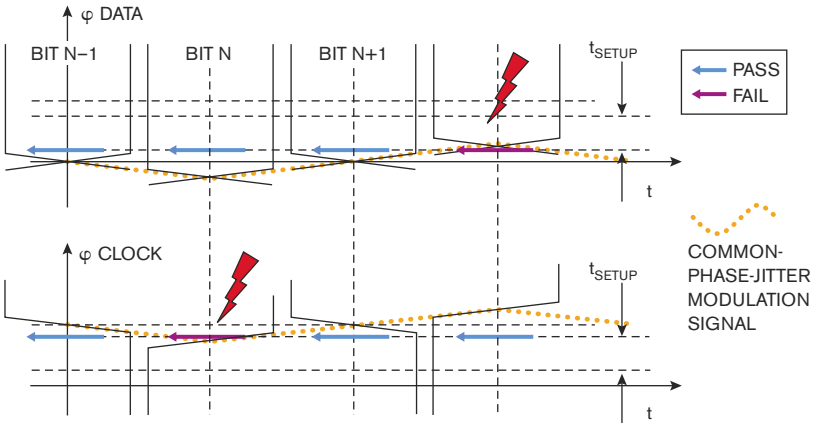

Figure 3 Data-crossover points and clock edges varying in time because of jitter may not occur at the right time for a tester with a fixed timing strobe to correctly capture them.

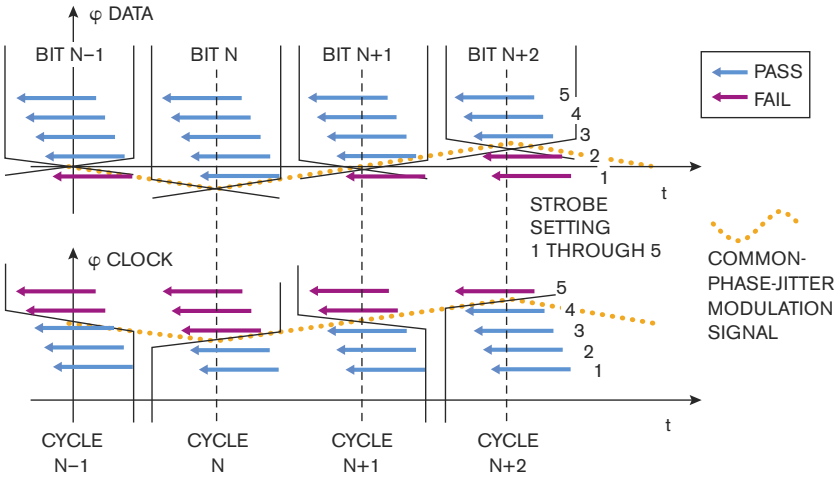

Figure 4 The use of multiple fixed strobes lets you find the strobe-phase locations that produce valid measurements of setup-and-hold time.

For the technique to work, the pattern must repeat, and the step width between strobes must be small enough for the ATE to find the required points. Even if the distortion varies from one test execution to another, the specified criterion is still valid. You can accept a cycle as passed if it passes with at least one strobe. Because different cycles can pass in different shots, you can accept the whole pattern if every cycle passes in at least one shot.

HIGH-VOLUME TESTING

Unlike characterization testing, production testing typically doesn't include measurement values. Instead, it uses pass/fail testing. The test time for a setup-and-hold-time pass/fail verification using the suggested algorithm includes multiple-pattern execution and loading and postprocessing of the error data. For cases with long patterns and wide search ranges, the resulting test times are too long for production. To achieve an acceptable test throughput, you need a certain level of ATE-hardware support.

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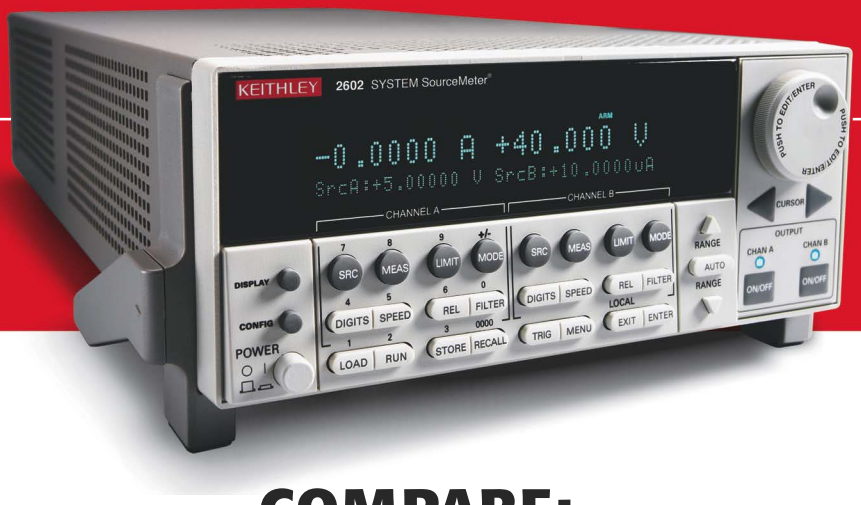

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as well as the ability to acquire large amounts of error information within a pattern run. You must also minimize the amount of data that you need to upload and process.

The Verigy V93000 tester-pin electronics that implements the test method lets you perform Boolean operations on the strobe results of the data and clock pins per cycle during upload. This ap-

SOURCE-SYNCHRONOUS INTERFACES

By using stable local clocks derived from a reference clock by means of a PLL (phase-locked loop), circuit designers have sidestepped many of the impairments that on-chip interconnects would introduce in devices with clock speeds greater than 1 GHz. Each local clock, part of a clock domain, services a set of local functions, such as I/O interfaces.

Figure A shows building blocks of a typical high-speed source-synchronous interface connecting two chips for one direction of data transmission. Source-synchronous interfaces typically split into several clock domains comprising a group of four to eight data lines and an associated source-synchronous clock.

Identical I/O drivers drive the data and the clock to ensure minimal relative skew and relative jitter between clock and data. On the receiver side, the source-synchronous clock latches the data. During regular operation, the interface can handle common-phase-jitter variations up to a certain bandwidth. Such source-synchronous-I/O technology aims to increase setup-and-hold-time margins, to enable high-speed synchronous traffic between devices, and to eliminate the need for precise clock and signal distribution.

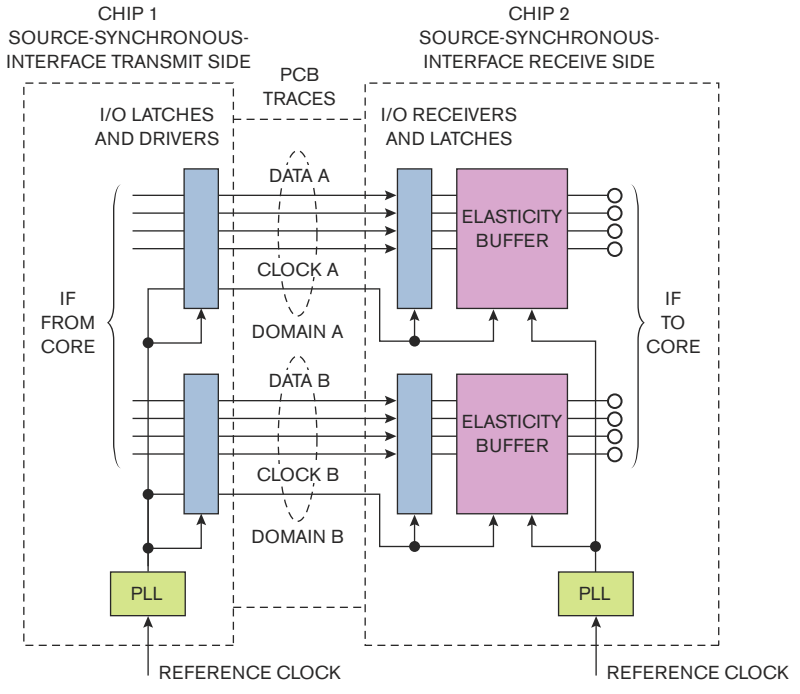

Figure A A source-synchronous interface uses PLLs to lock onto a reference clock, producing a local clock domain.

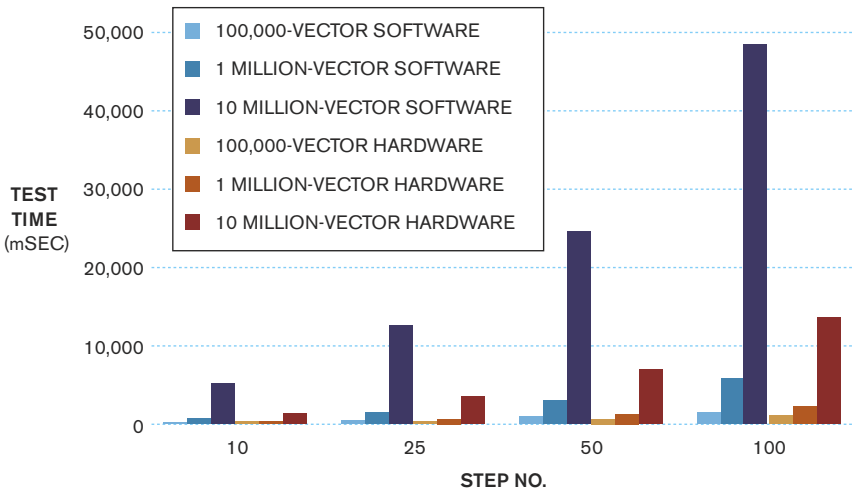

Figure 5 Data processed in hardware results in shorter tests.

proach reduces the amount of uploaded data that finally passes the serial link between the tester and the controller by a factor proportional to the sum of data and clock pins per source-synchronous domain.

An additional option is to avoid the data upload altogether and perform the data processing within the tester hardware, so that the system must communicate just the global pass/fail test results to the tester controller. Performing the postprocessing directly in the hardware eliminates the need to upload massive strobe-result data and improves throughput by several orders of magnitude.

Figure 5 illustrates the dependency of test time on the number of phase steps and the pattern length of the sample source-synchronous interface. Because test time translates into cost, you must determine a reasonable trade-off for the test coverage in pattern length and the number of phase steps. For characterization, even a pattern that is 10 million vectors long with 100 phase steps would give an acceptable test time when you use local data processing in the tester hardware.

Targeting use with standard ATE, this test methodology is an approach based on traditional capture-and-compare-pin electronics. You can scale the technique with your ATE hardware. The test method lets you perform both measurement (characterization) and validation (pass/fail) of timing parameters with fast throughput. You can also perform detailed analysis of failure mechanisms, including waveform shape, amplitude, and spectral content of common-phase drift and jitter. EDN

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AUTHOR'S BIOGRAPHIES

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EDN HANDS-ON PROJECT

Robots on the march

BY ROBERT CRAVOTTA • TECHNICAL EDITOR

Robots capture the imagination. With low-cost development platforms becoming more readily available, the opportunities for people to use robots for education and end applications continue to grow. The term "robot" is a tough beast to define, though, because people usually anthropomorphize these devices, thinking of them as servants or pets. Most people know a robot when they see one, but you would be hard-pressed to find a description that works all or even most of the time. For example, iRobot refers to its Roomba as a vacuuming robot, and many people have no trouble calling it a robot. On the other hand, many people have a harder time calling an autonomous automobile, such as those running in this year's DARPA (Defense Advanced Research Projects Agency) Urban Challenge, a robot. What is the defining difference between these functionally similar systems? More important, as a designer, is there a difference in the design approach and development resources that you need to build either of these types of systems? How does designing an embedded autonomous or semiautonomous subsystem, such as the braking- and traction-control systems on high-end automobiles, differ from designing what most people think of as a robot?

ROBOTICS IS GAINING MOMENTUM AS AN ENGINEERING DISCIPLINE. A VARIETY OF AVAILABLE PLATFORMS AND TOOLS SUPPORTS IT. THIS ARTICLE IS THE FIRST OF A TWO-PART HANDS-ON PROJECT EXPLORING THE TOPIC.

Fortunately, a growing number of design resources in the robotics community do not worry about such distinctions, and they are opening the world of robotics and autonomous subsystems to a wider range of people each day. This access is important; these types of systems are the results of cross-disciplinary teams of people with a range of general and domain-specific expertise. Robotic-development platforms provide these teams with a starting point that does not require them to be sensor-, mechanical-, and motor-control experts just to begin their project. As the software-development tools continue to mature for these systems, they will allow even higher momentum in domain experts' efforts in the specification, design, test, and deployment of these systems.

The first part of this hands-on project briefly describes the project and then focuses on the platforms and development tools I considered to implement the project. The second part, which is scheduled for *EDN*'s Feb 7, 2008, issue, will present the details of implementing the project with the chosen hardware and software platform. This hands-on project will attempt to meet multiple goals. The first goal is to expose you to the resources that are available to jump-start a development team's efforts to build autonomous systems, whether they are embedded or explicit and whether they are completely or only partially autonomous. Another goal is to explore the state of the art of these types of platforms and the development resources that support them; it is valuable to understand whether and to what extent these development resources are in or beyond an early-adopter level of maturity.

Another goal is to present the idea of sensing the world on a mobile platform rather than on a rigid platform. I've seen a lot of presentations, especially in vision sensing, in which the designers mount the sensor on a rigid framework and go to great lengths to remove the possibility of any motion during data capture. It seems that these types of systems are adopting greater computational loads to compensate for the data that a rigid, stationary platform cannot capture. When I was working on autonomous vehicles, my team purposely introduced motion into the sensing

scenario to help us to identify and filter out sensor anomalies and to make it easier to identify what we were trying to find. This project is a first cut at testing the feasibility of motion-assisted sensing to ultimately reduce growing computational workloads and to generate better data- and pattern-recognition results in sensing. For this project, I attempt to build a binaural-sensing system and demonstrate it as a dual-microphone, motion-assisted, sound-localizing robot. In other words, the robot will attempt to use two microphones pointing away from each other and coordinating with the robot's ability to move, to point at, and, ultimately, to identify the location of a sound source.

This project does not attempt to exhaustively identify all of the robotics-development resources that are available, because that community is continuously growing; rather, this project will identify a few mobile-robotics platforms that I considered for this project, along with the development resources that are available to support them. Check out the blog post in the *EDN* Embedded Processing channel, at www.edn.com/071203b1, to post and read about robotic-development resources that this write-up omits. Now, let's explore the platforms and development resources that I considered for this project.

PLATFORMS

Since 1990, iRobot has been delivering robots that perform tasks spanning from cleaning floors to disarming explosives. The company uses its proprietary Aware robot-intelligence systems to navigate around furniture and to search abandoned buildings. Versions of the iRobot Roomba that the company manufactured after October 2005 contain the iRobot Roomba SCI (serial-command interface), comprising electronics and software, that enables developers to control or modify their Roomba's behavior and remotely monitor its sensors. The Roomba SCI protocol provides a control link to a Roomba through its external serial port via a mini-DIN connector. The SCI includes commands to control all of the Roomba's actuators, such as the motors, LEDs, and speakers, and to request sensor data from all in-system sensors.

Figure 1 Robot manufacturer iRobot based its Create on the company's Roomba vacuuming robot, and it is available for educators, hobbyists, and developers to add their own hardware and software to control the platform.

AT A GLANCE

- A number of robotics-development platforms are available to designers.
- The development tools for robotics platforms are maturing; in some cases, they are several years behind the state of the art for traditional embedded-software-development tools.
- Reference designs and system-level development tools help speed prototyping by allowing designers to skip much of the custom building and integration that have been traditional in robotics projects.

In early 2007, the company released the iRobot Create, a preassembled mobile-robot platform with 32 built-in sensors, actuators, and serial interfaces that is available at prices starting at $129.99 (**Figure 1**). The company based Create on the core technology of the Roomba, and it is compatible with Roomba's rechargeable batteries, remote control, and other accessories. The platform includes an open-access payload bay; a 25-pin expansion port; and threaded mounting holes that can accommodate off-the-shelf sensors, actuators, and other third-party electronics, such as cameras, arms, and wireless connections to the robot.

Users can program the platform by downloading short scripts of numeric commands using a serial connection from a desktop computer or by loading programs to the command module. The processor in the command module is a 20-MHz, 8-bit Atmel ATMega168 microcontroller. The WinAVR set of open-source-development tools supports programming the command module in C or C++. The development tools include an editor, a compiler, and a downloader for the command module. Developers can also use Microsoft Robotics Studio, which the company released in December 2006, to program the robot. RoboDynamics' Roomba DevTools tools allow developers to control the Roomba platform from their computers using Bluetooth, USB, or serial interfaces.

The command-module manual includes low-level programming tips and examples (**Reference 1**). Programming tips include using 8-bit values whenever possible for calculations, avoiding floating-point arithmetic, and using integers and right shifts instead of division. One example of these tips is to write bit masks to registers or ports to clear, start, and read the ADC because there is currently no API (application-programming interface) for function calls. Another tip describes how to debounce a button input using a timer-delay function. Performing complicated autonomous controls will entail undergoing a substantial learning curve until iRobot adds an API framework that abstracts this layer, such as through Microsoft Robotics Studio, to the tool set.

Segway offers the RMP (robotic-mobility platform), which it based on the Segway PT (personal transporter); RMP is available in a durable package for human-scale-robotics applications (**Figure 2**). The Segway RMP includes configurations for moving heavy payloads in tight spaces over a variety of terrains. The Segway RMP motors can continuously produce 2 hp and can peak at 4 to 5 hp if necessary, which is sufficient to carry a human-sized payload. Segway RMP models are available in a variety of battery and tire/wheel combinations and offer a range as wide as 15 miles and payload capability of as much as 400 lbs. The Segway RMP runs on one to four NiMH (nickel-metal-hydride)- or Li-ion (lithium-ion)-battery packs. Any electrical-energy source that produces 52V can power a Segway RMP. You can outfit the Segway RMP with a compact gas generator to charge the batteries while in use.

The Segway RMP includes an onboard charging system, and the system is controllable through a USB or CAN (controller-area-network)-serial-bus interface. According to Segway, the USB

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electrical interface hides a CAN interface behind it because the company found that providing the USB front end greatly shortens the learning curve for developers interfacing with the platform. Developers can work directly at the CAN level if they desire. The company is considering adding other communication interfaces, such as Ethernet. The company is also considering improving the mechanical interfaces, including adding threaded holes for mounting brackets. Some models include support frames for custom sensing devices and computing hardware, casters for statically stable operation, or connection points for connecting Segway RMPs to each another. In lieu of mounting holes and brackets, some developers have successfully used industrial-grade Velcro to test and attach their prototype components to the platform.

The company's development support includes using open-source-development tools and access to multiple company-supplied algorithms for managing configurations of weight and balance on the platform. Segway and Microsoft recently announced support for the platform through Microsoft Robotics Studio. Microsoft Robotics Studio, an end-to-end Windows-based environment, supports the creation of robotics applications targeting hardware platforms that can host the .NET-based REST (representational-state-transfer) services-oriented runtime environment, such as Windows CE and Windows mobile devices. The runtime component supports the development of simulated robots; robots you control using a direct link to a desktop computer, such as through a serial port, USB, or Bluetooth link; and robots with an onboard control processor. The development environment also includes visual authoring and simulation tools. Several dozen companies, including iRobot, Lego, and Segway, have officially declared their support for the Microsoft Robotics Studio with their products (**Reference 2**).

According to the *Microsoft Robotics Studio User Guide*, the runtime environment comprises the CCR (concurrency-and-coordination-runtime) and the DSS (decentralized-software-services) components, and these components must adhere to the following set of requirements (**Reference 3**). It must be possible to monitor state and interact with components while an application is running. It must be possible to discover, create, terminate, and restart components while an application is running. It must be possible to concurrently deal with inputs from multiple sensors and to orchestrate such inputs as tasks without the risk of unintended interference between the tasks. It must be possible to handle both autonomous and controlled robotics applications both locally and remotely across the network. The runtime must be lightweight enough to allow execution in a wide variety of environments. The application environment must be extensible and flexible enough to accommodate interaction with a wide variety of hardware and software environments.

Figure 2 Segway based the RMP (robotic-mobility platform) on the company's personal-transporter product, and it is available in several configurations to support different payload and terrain scenarios.

Figure 3 National Instruments offers a version of LabView to support development for Lego's Mindstorm NXT.

The CCR supports asynchronous and concurrent operation through a message-oriented-programming model that can automatically exploit parallel hardware and coordinate messages without the use of manual threading, locks, or semaphores. This approach enables designers to build more loosely coupled software modules or components. The self-contained CCR .NET DLL is accessible from any language targeting the .NET 2.0 CLR (Common Language Runtime). Microsoft built the DSS runtime on CCR, and the DSS does not rely on any other components in Microsoft Robotics Studio. It provides a hosting environment for managing services and a set of infrastructure services that you can use for service creation, discovery, logging, debugging, monitoring, and security. The DSS supports a lightweight, service-oriented application model that combines aspects of the traditional REST Web-based architecture with pieces of the Web Services architecture. DSS defines an application model that builds on the REST model by exposing services through their state and a uniform set of operations over that state but extends the application model of HTTP (hypertext-transfer protocol) by adding structured data manipulation, event notification, and service composition.

The primary goal of DSS is to provide interoperability between services regardless of whether these services are running within the same node or across the network. DSS uses HTTP and DSSP (Decentralized Software Services Protocol) as the foundations for interacting with services. The lightweight, SOAP (simple-object-access-protocol)-based DSSP supports the manipulation of a structured state and an event model, which changes to the structured-state drive. You use DSSP for manipulating and subscribing to services as a state-driven application model.

The Microsoft VPL (Visual Programming Language) graphical authoring development environment uses a data-flow rather than a control-flow programming model. A VPL data flow consists of a connected sequence of activities, which the flow represents as blocks with inputs and outputs that you can connect to other activity blocks. Activities can represent prebuilt services, data-flow control, functions, or other code modules; activities can also include compositions of other activities. VPL targets novice programmers, but the programming language may appeal to advanced programmers for rapid prototyping or code development.

The Robotics Studio simulation run-

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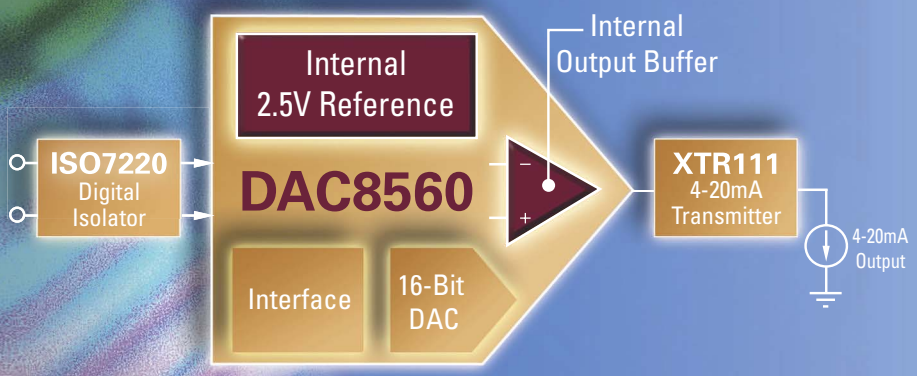

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DAC8564	Ultra-low glitch, 2ppm/°C internal reference, quad, POR to zero	16	4	SPI	8	Int	4	TSSOP-16	$11.25
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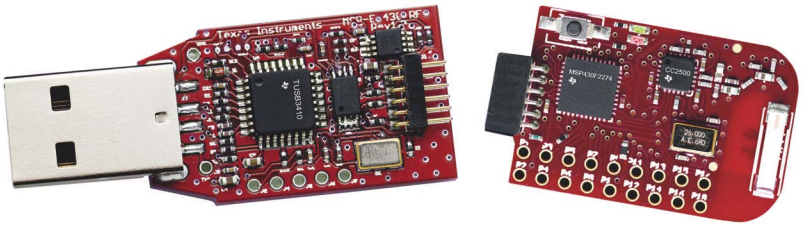

Figure 4 Texas Instruments' eZ430-RF2500 development tool was an extension-board candidate in part because of its modular approach to wireless communications.

time comprises the simulation-engine service, managed-physics-engine wrapper, native-physics-engine library, and software components that interface with the physics engine and the rendering engine to represent the hardware and physical objects in the simulated world. The simulation-engine service handles rendering entities and progressing the simulation time for the physics engine. It tracks the entire simulation's state and provides a service/distributed front end to the simulation. The managed-physics-engine wrapper abstracts the user from the low-level physics-engine API to provide a managed interface to the physics simulation. The native-physics-engine library enables hardware acceleration through Ageia PhysX Technology, which supports hardware acceleration through the Ageia PhysX Technology processor that is available as PhysX Accelerator add-in cards for desktop computers. A number of predefined entities come with the Microsoft Robotics Studio, and they expose high-level interfaces to emulate hardware and hide the use of physics APIs.

Developers can choose to interact only with the managed-physics-engine API without any visualization. To simplify inspection, debugging, and persistence of state of simulation code, however, Microsoft recommends that developers always use the simulation-engine service and define custom entities that disable the rendering. The rendering engine uses the programmable pipeline of graphics-accelerator cards, conforming to DirectX9 pixel/vertex-shader standards.

Lego's Mindstorms NXT is the latest generation of the company's robotic-tool sets that began with the Robotics Invention System that has been commercially available since 1998; the NXT became available in August 2006. A growing list of built-in resources, third-party resources, and professional-grade-development tools, such as National Instruments' LabView tool kit for Lego, support this platform. This plethora of support belies a possible first impression that the NXT is merely a toy (**Figure 3**). In fact, Lego's building-block approach to NXT gives the platform the mechanical flexibility that may make it suitable for quick prototyping and exploring multiple physical configurations for sensors and motion components.

The NXT brick relies on a 32-bit ARM7 (www.arm.com) processor to provide the autonomous controller for the platform. The basic system includes three servo motors with built-in rotation sensors for precise control, an ultrasonic sensor to detect motion, a sound sensor that supports sound-pattern and tone recognition, a light sensor that detects colors and light intensity, a touch sensor, and USB 2.0 and Bluetooth wireless interfaces to support development and the integration of third-party resources. Visiting the Mindstorms Web site reveals a rich ecosystem of user resources and development, including the open-source NXT firmware-, software-, and hardware-development kits and a Bluetooth-development kit. The suggested retail price of the basic system at release was $249.99.

The use of LabView as a development

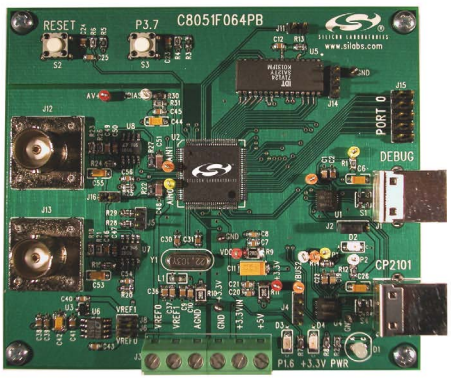

Figure 5 Silicon Labs' C8051F064EK evaluation kit was an extension-board candidate in part because of its dual ADC that could simultaneously take samples from two microphones.

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tool for the NXT coincided with the release of the NXT platform last year, and, along with the increasing number of platforms that Microsoft Robotics Studio supports, these tool suites potentially portend an explosion of support and tool announcements. At one level, this explosion would open programming-robotics platforms to a larger group of developers through higher level abstractions. At another level, it would enable higher productivity and the ability to leverage the efforts of third-party developers into increasingly complex and relevant robotics designs. It would achieve these goals by providing a robust mechanism for developers to encapsulate, protect, and distribute their designs for robotic subsystems. Using the LabView tool kit to program the NXT requires LabView 7.1, 8.0, or 8.20; creating native blocks for the NXT software requires LabView 7.1.

The LabView graphical-development environment includes a built-in compiler, supports real-time data-acquisition and instrument control, and includes graphical presentation tools for creating control and test applications. It supports the features of a general-purpose programming environment, such as data structures, looping structures, event handling, and object-oriented programming, through a data-flow-programming model that allows the flow of data between nodes, not sequential lines of text, to determine the execution order of the code. This approach allows developers to create block diagrams that capture multitasking or multithreaded components and can execute multiple operations in parallel if the appropriate hardware is available.

Developers can extend the functions of LabView with add-ons that address software optimization; data management and visualization; and deployment to various hardware targets, including FPGAs. Other add-ons address signal processing and analysis; automated test, image acquisition, and machine vision; and control-design and simulation industrial control. Hundreds of third-party add-ons include those interfacing with third-party tools, such as the MathWorks' Simulink environment, to model and simulate designs.

EXTENSIBILITY

A common theme across all of these platforms is the support for extensibility, not just for custom and third-party software modules, but also for hardware interfaces and subsystems. Each of these platforms offers the mobility I desired for this hands-on project, but I would need to extend these platforms with hardware and software to add a binaural-sensing capability and for directing the movement of the platform in response to the audio inputs.

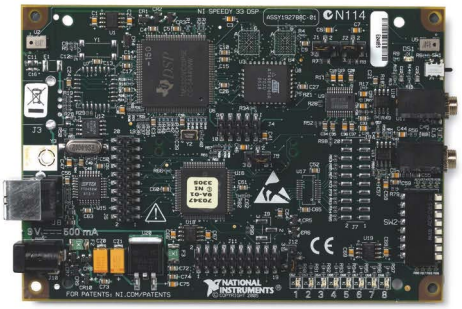

Figure 6 National Instruments' Speedy 33 signal-processing module includes dual integrated microphones and drivers and virtual instruments to work with the sampled data.

Unlike the iRobot Create and the Lego NXT, the Segway RMP includes the ability to sense its orientation and inertial motion, which I believe will be essential for performing sound localization in production units. However, this hands-on proof-of-concept project aims to find out whether coupling even coarse-level motion control with binaural sensing makes the problem of sound localization more tractable. Additionally, at this point, the long learning curve for interfacing the hardware components and creating the software controls for the RMP seemed like a hefty price to pay for using the RMP just for a prototype proof-of-concept project. This problem left the Create and the NXT as platform candidates.

My initial focus was on the iRobot platform because I had acquired a Roomba for use in an earlier project (**Reference 4**) and because the Roomba has algorithms for navigating around a room with uncertain placement of objects. The challenge would be to find modules that I could quickly set up to collect the audio inputs and issue commands to and receive responses from the Roomba controller. I found two evaluation platforms that could act as candidates for the audio-sensing and high-level-controller subsystem for the project.

One of these platforms, the Texas Instruments eZ430-RF2500 development tool, includes two USB-stick-sized development boards, which support a wireless connection between them (**Figure 4**). The wireless link appeals to me because I have for years wanted to do a project with one, and it appears that adding wireless to a design is finally approaching the level of adding a module to the system instead of building one from components. One of the boards gets its power from the USB connection with a host computer, and the other connects to and accepts power from a battery case. The boards host a 16-MHz, 16-bit MSP430F2274 microcontroller, which provides sufficient processing capacity and a 10-bit, 200k-sample/sec ADC, which is fast enough to acquire the audio inputs.

The other platform, the C8051F064-EK evaluation kit from Silicon Labs, features a 25-MIPS, 8-bit C8051F064 microcontroller with dual 16-bit, 1M-sample/sec ADCs to acquire simultaneous samples from both of the audio inputs (**Figure 5**). The evaluation board can accept power through the USB link with a host computer and includes a BNC and front-end circuitry to condition the analog signals for each of the two analog inputs. However, to use either of these boards, I would have to build hardware interfaces and software drivers for the microphones and to communicate through the Roomba's serial port.

While I was exploring using LabView with the Lego NXT with National Instruments, I found out that an engineer at National Instruments had recently used an NXT in a demonstration application similar to an electronic "sheep dog," which would perform an action, such as turn left or right, stop, or go forward, based on the sound it heard. This feature differs from performing motion-assisted sound localization, but knowing the details of that project could allow me to use it as a reference design and save me valuable time in configuring a setup to perform this hands-on project.

Another reason that I chose the NXT system was the immediate availability of already-identified and appropriate modules that I could interface to the NXT system. Coupling National Instruments' Speedy 33, a Texas Instruments TMS320VC33-based DSP board, with the LabView DSP module and a sensor prototype board from HiTechnic resulted in a configuration that combined all of the appropriate hardware to do this project. The Speedy 33 integrates two microphones that are approximately 5 in. apart, with 48-kHz sampling, and, with the LabView DSP module, provides access to a library of data-acquisition and -analysis virtual instruments for time- and frequency-domain signal processing (**Figure 6**). The HiTechnic prototype board provides a physical link between the Speedy 33 and the NXT and also provides a logical mapping into the NXT's sensor-memory model.

Part 2 of this hands-on article, scheduled for Feb 7, 2008, will delve into the details of working with the NXT platform and the development resources to accomplish sound localization with motion-assisted binaural sampling. If time and space allow, I will also try out and share the experience with the Microsoft Robotics Studio modeling and simulation facilities. EDN

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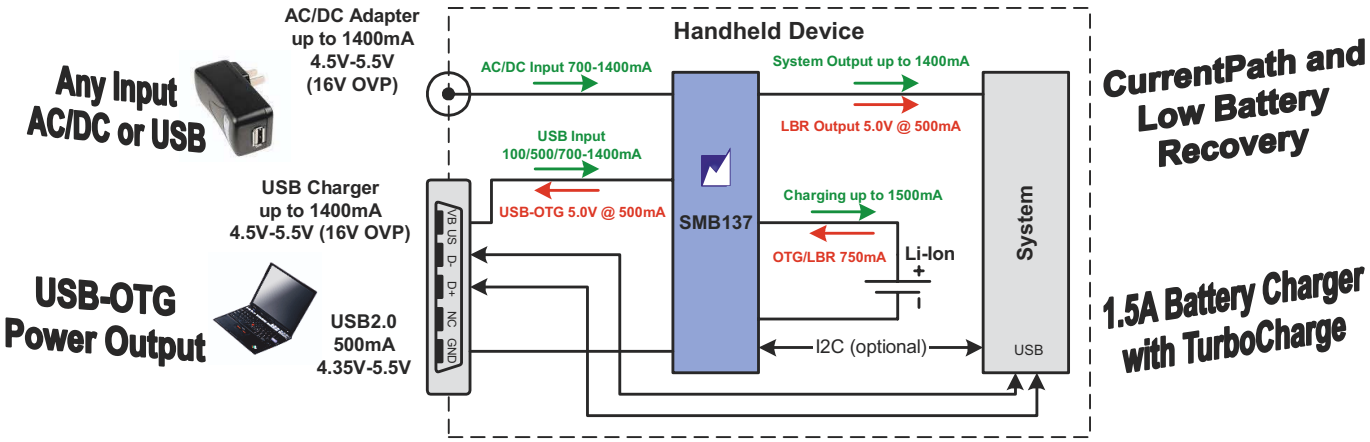

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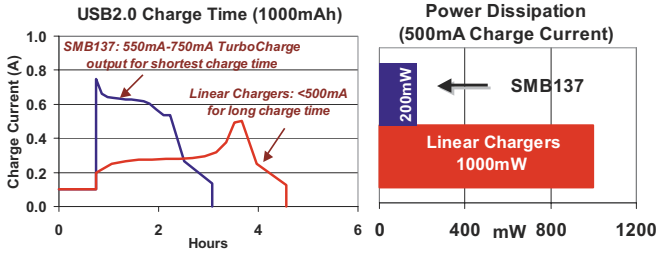

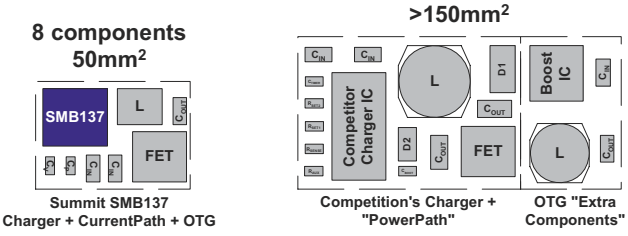

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Coding SPI software

THE SPI REQUIRES THREE WIRES FOR DATA TRANSFER PLUS A DEVICE-SELECT SIGNAL. DESIGNERS CAN IMPLEMENT PERIPHERAL COMMUNICATIONS USING PROCESSOR-BASED HARDWARE OR THE SOFTWARE ROUTINES THAT THIS ARTICLE PRESENTS.

A variety of peripheral devices in modern embedded systems, such as EEPROMs, ADCs, DACs, real-time clocks, thermal sensors, and display and communication controllers, have synchronous serial interfaces. These interfaces' main benefit is that only a few wires connect peripherals to a processor. Some cases require serial peripherals—for instance, when the system processor has a low I/O-pin count. While communicating with a device through a synchronous serial interface, data and a timing clock transmit over separate wires. The processor acts as the master, and a peripheral device acts as the slave. Only the master can initiate communications and generate the timing clock. The three main synchronous-serial-interface standards are Microwire from National Semiconductor (www.national.com), SPI (serial-peripheral-interface) from Motorola (www.motorola.com), and I²C (inter-integrated circuit) from Philips (www.philips.com). Numerous proprietary synchronous serial interfaces exist, as well. Software in C enables a microcontroller from the Intel (www.intel.com) MCS-51 family to access SPI peripherals. This article explains how you can implement this software.

People often refer to SPI as a three-wire interface, but the interface bus comprises more than three wires. The three wires carry input data to that slave and output data from the slave and the timing clock. The developers from Motorola labeled the three wires MOSI (master out/slave in), MISO (master in/slave out, and SCK (serial clock). Multiple slaves can share these wires (**Reference 1** and **Figure 1**). The SPI slave also has a select input SS (slave select), and the master must generate a separate select signal for each slave in the system; a low-level signal selects most of the available slaves. Occasionally, a select signal also initiates a data transfer. If only one slave exists, you can sometimes permanently force its select input to an active level. The slave's data sheet specifies the maximum clock-frequency value. The manufacturers of slave devices also use equivalent labels for bus lines. MOSI is equivalent to SI (slave in) or DI (data in). MISO is equivalent to SO (slave out) or DO (data out), SCK approximates SCLK (which also stands for serial clock), and SS is approximately equivalent to CS (chip select). A high-level signal selects some serial devices.

LISTING 1 CONFIGURATION OF THE SPI PORT

```
#define uchar unsigned char

void SPI_configuration(uchar configuration)
{
  P1 |= 0xF0;              /* programming SPI pins high */
  SPCR = configuration;
}
```

LISTING 2 SENDING AND RECEIVING A BYTE

```
#define SPIF 0x80          /* SPI interrupt flag in SPSR */

uchar SPI_transfer(uchar byte)
{
  SPDR = byte;             /* byte to send */
  while(!(SPSR & SPIF));   /* wait until end of transfer */
  return(SPDR);            /* received byte */
}
```

SPI OPERATION

SPI's developers based its operation on the use of two 8-bit shift registers (**Figure 2**). While the master communicates with the selected slave, the two devices' shift registers connect in a ring, so both devices always simultaneously send and re-

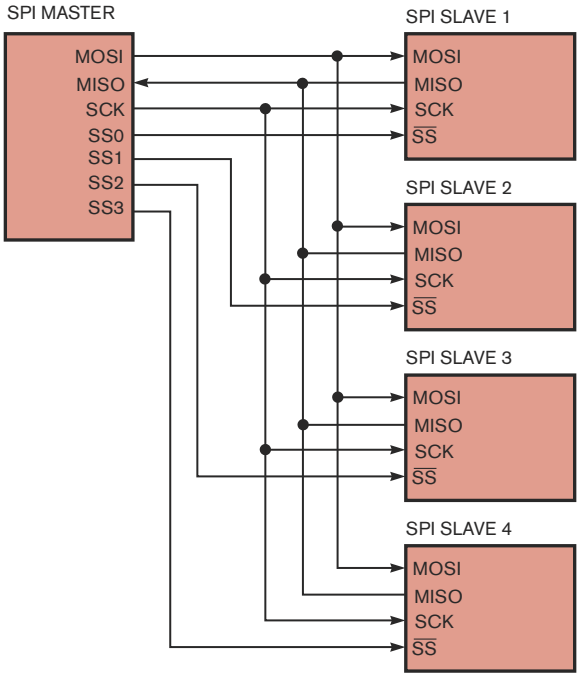

Figure 1 An embedded system comprises a few SPI peripherals under the control of one master.

ceive. If the dialogue between them requires only half-duplex communication, each device discards the bytes it received in the transmitting phase and generates dummy bytes in the receiving phase. A pair of parameters, CPOL (clock polarity) and CPHA (clock phase), defines the SPI mode. These parameters are binary digits, so there are four possible modes. CPOL selects the level of the SCK line before and after byte transfer. CPHA determines the edges of the clock on which a slave latches input-data bits and shifts out bits of output data. A master/slave pair must use the same mode to communicate. **Figure 3** presents the timing diagrams of a byte transfer in all modes.

Assume that the clock edges are numbered from one. When the CPHA equals zero, input-data bits latch onto each odd clock edge, and output-data bits shift out onto an even clock edge. The select signal initiates a byte transfer, and the first bit of output data is available after activating this signal. When a byte transfer terminates, the select line must deactivate. When CPHA equals one, input-data bits latch onto each even clock edge, and output-data bits shift out onto each odd clock edge. The first clock edge indicates the start of a byte transfer. The SS line may remain at its active level between transfers of successive bytes; a slave considers a byte transfer complete after the eighth bit latches. If there is one slave in the system, its select input may sometimes permanently remain at the active level. In 0,0 and 1,1 modes, input-data bits latch on the rising clock edges, and output-data bits shift out on the falling clock edges. The remaining modes use falling and rising clock edges.

Numerous available slave devices support both 0,0 and 1,1 modes. You access these devices using commands that often require the transfer of multiple bytes. You must select these devices before transfer of each command and deselect them after transfer of each command.

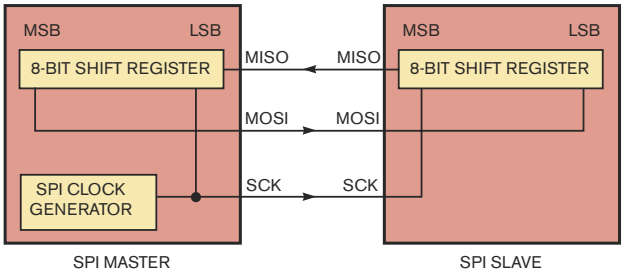

Figure 2 Each SPI device contains an 8-bit shift register. The registers of the master and selected slaves connect in a ring, allowing full-duplex communication to take place.

PORT IMPLEMENTATIONS

Motorola first included a hardware-SPI port in the 68HC11 family of microcontrollers and then extended the port to many other microcontrollers. Microcontrollers from other manufacturers, such as Atmel's (www.atmel.com) AT89S8253, also support SPI (**Reference 2**). This microcontroller is an extended 8052 device with flash program memory, which you can reprogram in a target system through SPI. Its SPI port provides master or slave operation, normal or enhanced mode, programmable-SPI mode, MSB (most-significant-bit)- or LSB (least-significant-bit)-first data transfer, four programmable SCK frequencies, an end-of-transmission interrupt flag, write-collision flag protection, a double-buffered receiver, a double-buffered transmitter in enhanced mode, and a wake-up from idle mode in slave mode.

In normal mode, three SFRs (special-function registers) control access to the port (**Figure 4**), and the microcontroller's data sheet describes those registers. **Listings 1** through **7**, written in Keil C51, illustrate the use of the port (**Reference 3**). The header file, which comes with the compiler, includes a list of the addresses of SFRs available on the AT89S8253. **Listing 1** shows the routine configuring the SPI port. If you enable the SPI port, it uses pins of the high nibble of Port 1 (P1.4 through SS/, P1.5 through MOSI, P1.6

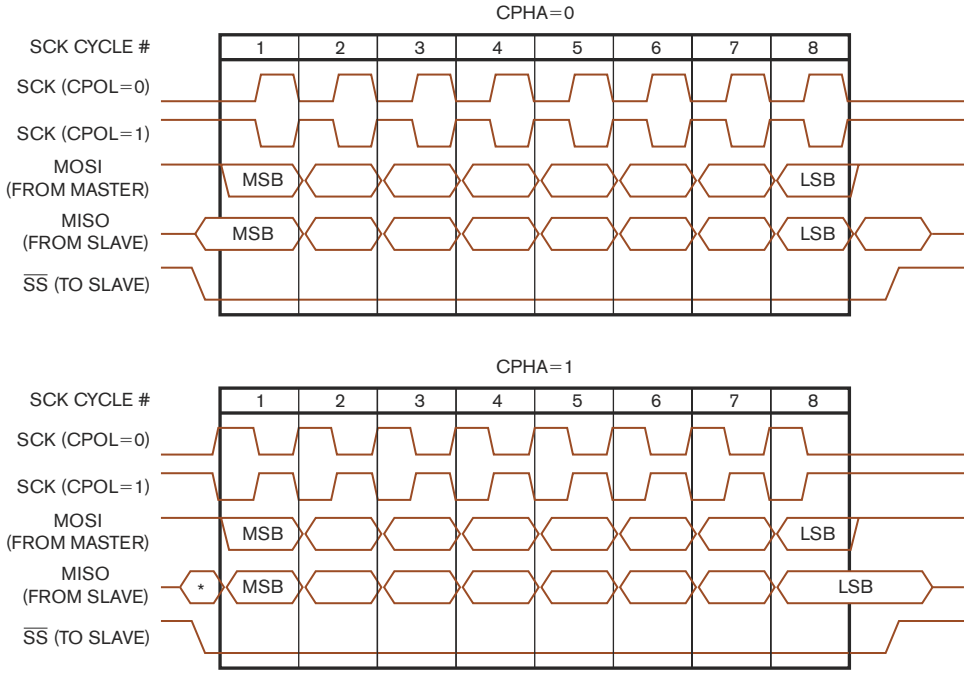

Figure 3 A master/slave pair must use the same mode to communicate. The timing diagrams of a byte transfer in all modes yield these timing profiles.

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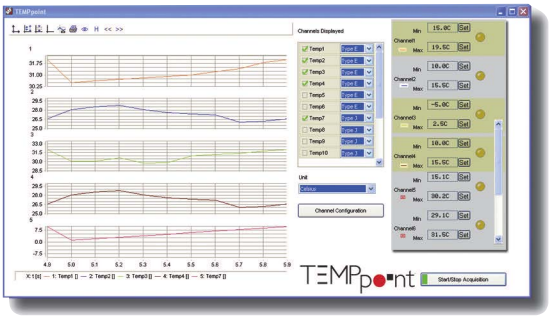

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LISTING 3 BIT-BANGING SPI-TRANSFER ROUTINES

```
sbit MOSI = P1 ^ 0;     /* this declaration assigns pins of */
sbit MISO = P1 ^ 1;     /* Port 1 as SPI pins */
sbit SCK  = P1 ^ 2;

/* a byte transfer in (0,0) mode */

uchar SPI_transfer(uchar byte)
{
uchar counter;

  for(counter = 8; counter; counter--)
  {
    if (byte & 0x80)
      MOSI = 1;
    else
      MOSI = 0;
    byte <<= 1;
    SCK = 1;     /* a slave latches input data bit */
    if (MISO)
      byte |= 0x01;
    SCK = 0;     /* a slave shifts out next output data bit */
  }
  return(byte);
}

/* a byte transfer in (1,1) mode */

uchar SPI_transfer(uchar byte)
{
uchar counter;

  for(counter = 8; counter; counter--)
  {
    if (byte & 0x80)
      MOSI = 1;
    else
      MOSI = 0;
    SCK = 0;         /* a slave shifts out output data bit */
    byte <<= 1;
    if (MISO)
      byte |= 0x01;
    SCK = 1;         /* a slave latches input data bit */
  }
  return(byte);
}
```

LISTING 4 BIT'S ORDER INVERSION IN A BYTE

```
uchar inverse(uchar byte)
{
uchar mask = 1, result = 0;

  while(mask)
  {
    if (byte & 0x80)
      result |= mask;
    mask <<= 1;
    byte <<= 1;
  }
  return(result);
}
```

through MISO, and P1.7 through SCK). Atmel recommends that you set these pins high before writing to the control register; otherwise, the SPI port may not operate correctly. You must program the SPI pins in **Listing 1** if you need to reconfigure the port while the microcontroller executes its program. You can omit this operation if configuration occurs only once because a hardware reset sets the SPI pins high.

The AT89S8253 can act as an SPI master or an SPI slave, but this article considers only master operation. **Listing 2** presents a routine that sends and receives a byte through the SPI port. Writing to the SPI-data register initiates a transfer, starts the clock generator, and shifts out the output byte on the MOSI pin. Simultaneously, a byte from a slave shifts into the SPI-data register. The While loop executes until you set the SPI-interrupt flag in the SFR, which indicates the end of transfer. You clear this flag by reading the status register by setting the SPI-interrupt-flag bit and then accessing the data register.

SPCR-SPI CONTROL REGISTER (ADDRESS D5H)

SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0

SPSR-SPI STATUS REGISTER (ADDRESS AAH)

SPIF	WCOL	LDEN	—	—	—	DISSO	ENH

SPDR-SPI DATA REGISTER (ADDRESS 86H)

SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0

Figure 4 SFR registers control the hardware-SPI port of the AT89S8253 microcontroller in normal mode.

TABLE 1 COMMAND SET FOR THE CAT25040

Command	Command's format (a=address bit; d=data bit)			Operation
WREN	00000110	–	–	Enable write operations
WRDI	00000100	–	–	Disable write operations
RDSR	00000101	$d_7 \div d_0$[1]	–	Read status register
WRSR	00000001	$d_7 \div d_0$	–	Write status register
READ	$0000a_8011$	$a_7 \div a_0$	$d7 \div d_0$[1]	Read data from memory
WRITE	$0000a_8010$	$a_7 \div a_0$	$d7 \div d_0$[2]	Write data to memory

[1] Data bits transfer on MISO line; a single read command can read any number of bytes.
[2] A single write command can write as many as 16 bytes.

You can generate an interrupt request after the transfer completes, but this feature is more useful in slave operation. Writing to the SPI-data register during a transfer sets the WCOL (write-collision)-flag bit in the SPI-status register. This operation has no effect, and the result of reading the data register may be incorrect. Reading the status register with WCOL bit set, followed by accessing the data register, clears this flag. Using the SPI-transfer routine only to communicate with slave devices prevents collisions.

Microcontrollers without hardware support for SPI also can communicate with SPI devices, because it is feasible to perform a "bit-banging," an all-software port implementation. Any microcontroller's general-purpose-I/O pins can serve as SPI pins. Most slave devices support both 0,0 and 1,1 SPI modes; to communicate with these devices, you can use one of the equivalent SPI-transfer routines in **Listing 3**.

If a slave device supports only one mode, you must ensure that you forced the SCK line to the proper level before selecting the device. The hardware-SPI port features MSB- or LSB-first data transfer, and bit-banging routines always send MSB first. If a slave in the system requires LSB first, you can inverse the bits' order in a byte that passes to the SPI-transfer

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routine and a byte that this routine returns. The routine in **Listing 4** performs this inversion. If you compare all versions of the SPI-transfer routine with respect to code-memory occupation and achievable bit rates in both SPI-port implementations, you will find that the routine that uses hardware-based SPI occupies 10 bytes of code memory, and the bit-banging routines occupy 29 bytes each if you pass in the parameters and place the local variables in the register. The AT89S8253 has one- and two-times clock options, and the machine cycles for these clocks take 12 and six oscillator periods, respectively. Maximum SCK frequency is f_{OSC}/N, where f_{OSC} is the oscillator frequency and N is 4 in the one-times mode and 2 in the two-times mode. Because it takes one clock cycle to transfer one data bit, the maximum bit rate equals f_{OSC}/N bps. A byte transfer using the bit-banging routine takes a minimum of 111 machine cycles, so the maximum bit rate is $8/(111\times t_{CYCLE})$ bps, where t_{CYCLE} is the cycle duration. For example, a classic 8051 microcontroller with a 12-MHz crystal can transmit SPI data at approximately 72 kbps.

SERIAL EEPROM

Designers often use EEPROMs as slave devices in an inexpensive approach to storing data in nonvolatile memory. Several manufacturers offer serial EEPROMs in capacities of 1 to 64 kbits or more. **Listing 5** presents software that allows access to a Catalyst Semiconductor (www.catsemi.com) CAT25040 device or equivalent (**Reference 4**). The CAT25040 provides 512 bytes of nonvolatile memory with 100-year data retention.

LISTING 5 CAT25040 READ OPERATIONS

```
#define uint  unsigned int
#define RDSR  5            /* codes of commands         */
#define READ  3

sbit EEPROM_SEL = P1 ^ 4;  /* select pin for the EEPROM */

uchar EEPROM_byte_read(uint address)
{
uchar byte;

  EEPROM_SEL = 0;
  SPI_transfer((address >> 8) ? (READ | 8) : READ);
  SPI_transfer((uchar)address);
  byte = SPI_transfer(0xFF);
  EEPROM_SEL = 1;
  return(byte);
}

void EEPROM_sequential_read(uint address, uchar
*destination,
                            uint size)
{
  if (size)
  {
    EEPROM_SEL = 0;
    SPI_transfer((address >> 8) ? (READ | 8) : READ);
    SPI_transfer((uchar)address);
    for( ; size; size--, destination++)
      *destination = SPI_transfer(0xFF);
    EEPROM_SEL = 1;
  }
}

uchar EEPROM_status_read(void)
{
uchar status;

  EEPROM_SEL = 0;
  SPI_transfer(RDSR);
  status = SPI_transfer(0xFF);
  EEPROM_SEL = 1;
  return(status);
}
```

It provides 1 million write/erase cycles and supports 0,0 and 1,1 SPI modes with a maximum SCK frequency of 10 MHz. In addition to the SPI pins, the CAT25040 has two other pins. The Hold pin enables the master to pause communication with the

LISTING 6 CAT25040 WRITE OPERATIONS

```
#define WREN  6          /* codes of commands */
#define WRSR  1
#define WRITE 2

bit EEPROM_byte_write(uint address, uchar byte)
{
  EEPROM_SEL = 0;        /* writing enable */
  SPI_transfer(WREN);
  EEPROM_SEL = 1;

  EEPROM_SEL = 0;        /* write data     */
  SPI_transfer((address >> 8) ? (WRITE | 8) : WRITE);
  SPI_transfer((uchar)address);
  SPI_transfer(byte);
  EEPROM_SEL = 1;

  return(programming_status());
}

bit EEPROM_page_write(uint address, uchar *source,
                      uchar size)
{
  if (!size || (uchar)(((uchar)address & 15) + size) > 16)
    return(0);           /* invalid number of bytes or they would
                            not occupy adjacent locations */

  EEPROM_SEL = 0;      /* writing enable */
  SPI_transfer(WREN);
  EEPROM_SEL = 1;

  EEPROM_SEL = 0;      /* write data     */
  SPI_transfer((address >> 8) ? (WRITE | 8) : WRITE);
  SPI_transfer((uchar)address);
  for( ; size; size--, source++)
    SPI_transfer(*source);
  EEPROM_SEL = 1;

  return(programming_status());
}

bit EEPROM_status_write(uchar status)
{
  EEPROM_SEL = 0;       /* writing enable */
  SPI_transfer(WREN);
  EEPROM_SEL = 1;

  EEPROM_SEL = 0;       /* write status   */
  SPI_transfer(WRSR);
    SPI_transfer(status);
    EEPROM_SEL = 1;

    return(programming_status());
  }
```

LISTING 7 PROGRAMMING-STATUS ROUTINE

```
#define RDY 1          /* READY bit in the status register
*/

bit programming_status(void)
{
uchar counter;

  for(counter = 16; counter; counter--)
  {
    delay(84);         /* about 0.5 ms, when fosc = 12 MHz
*/
    if (!(EEPROM_read_status() & RDY))
      return(1);       /* OK      */
  }
  return(0);           /* failure */
}

/* suspension of program execution for (number * 6) + 1
   machine cycles */

void delay(uchar number)
{
  while(number--);
}
```

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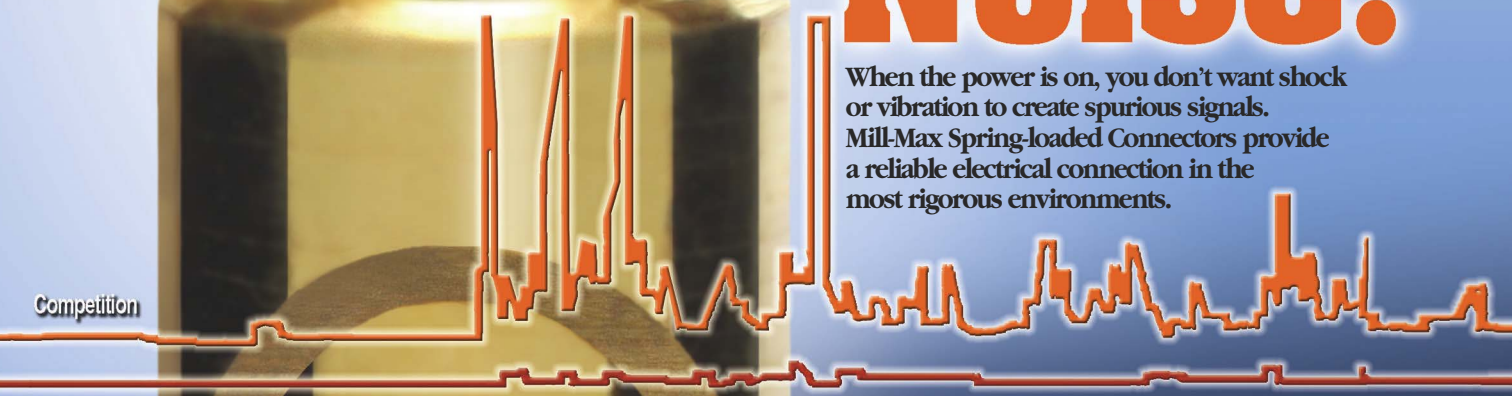

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EEPROM if another slave requires urgent servicing. The WP (write-protect) pin allows enabling and disabling writes to the memory array and the memory's status register. Enabling writing allows two or more nonvolatile bits in the status register to protect all or a portion of the memory array. In addition, you must set a write-enable latch before any write operation occurs.

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You access the CAT25040 using six commands (**Table 1**). The first byte is the command's code. The codes of the read and write commands contain the MSB of the location's address. You must select the memory before the transfer of each command and deselect it after the transfer. **Listing 5** presents sample routines performing read operations. After the EEPROM receives the read command's code and address, the address loads into an address counter, and the memory responds with a byte stored at the given address. The master can read the sequence of data by continuing to provide clocking. The address counter automatically increments to the next address after each byte shifts out. When the EEPROM reaches the highest address, the next address equals zero. The sequential read is a convenient way to get multibyte values from the EEPROM. You use the separate routine to read the status of the memory.

Listing 6 provides sample routines performing write operations. Before any write occurs, the master must set the write-enable latch in the EEPROM by issuing the write-enable command. Next, the master sends the write command's code, followed by the address, which loads into the address counter, and the data to write. The master can write as many as 16 bytes—a page write—by continuing to provide clocking. Compatible EEPROMs offer different page sizes. The address counter's bits constitute a page number, and the remaining bits address bytes within the page. After the EEPROM receives each byte, it increments only the address within the page. When the EEPROM reaches the highest address, the next address is zero, and if the clock continues, it may overwrite other data. To prevent this situation, the EEPROM page-write routine checks whether all bytes to write will occupy an area of consecutive addresses. If not, the routine does not issue a write command. A separate routine writes the memory's status register.

When the master deselects the EEPROM after issuing a write command, the memory enters the internal programming cycle. This cycle takes as long as 5 msec. The memory then ignores all commands except the read-status-register command. The LSB of the memory's status register indicates whether the programming cycle is in progress or complete. The programming-status routine checks this bit every 0.5 msec (**Listing 7**). The number of checks is limited; exceeding the limit indicates failure of the write operation. After the end of the programming cycle, the device is write-protected.

A range of serially accessed peripheral devices finds use in embedded systems. Connecting them to a processor requires a few wires. Such devices typically include a synchronous interface, of which the SPI is one of the most popular (**references 5** and **6**).EDN

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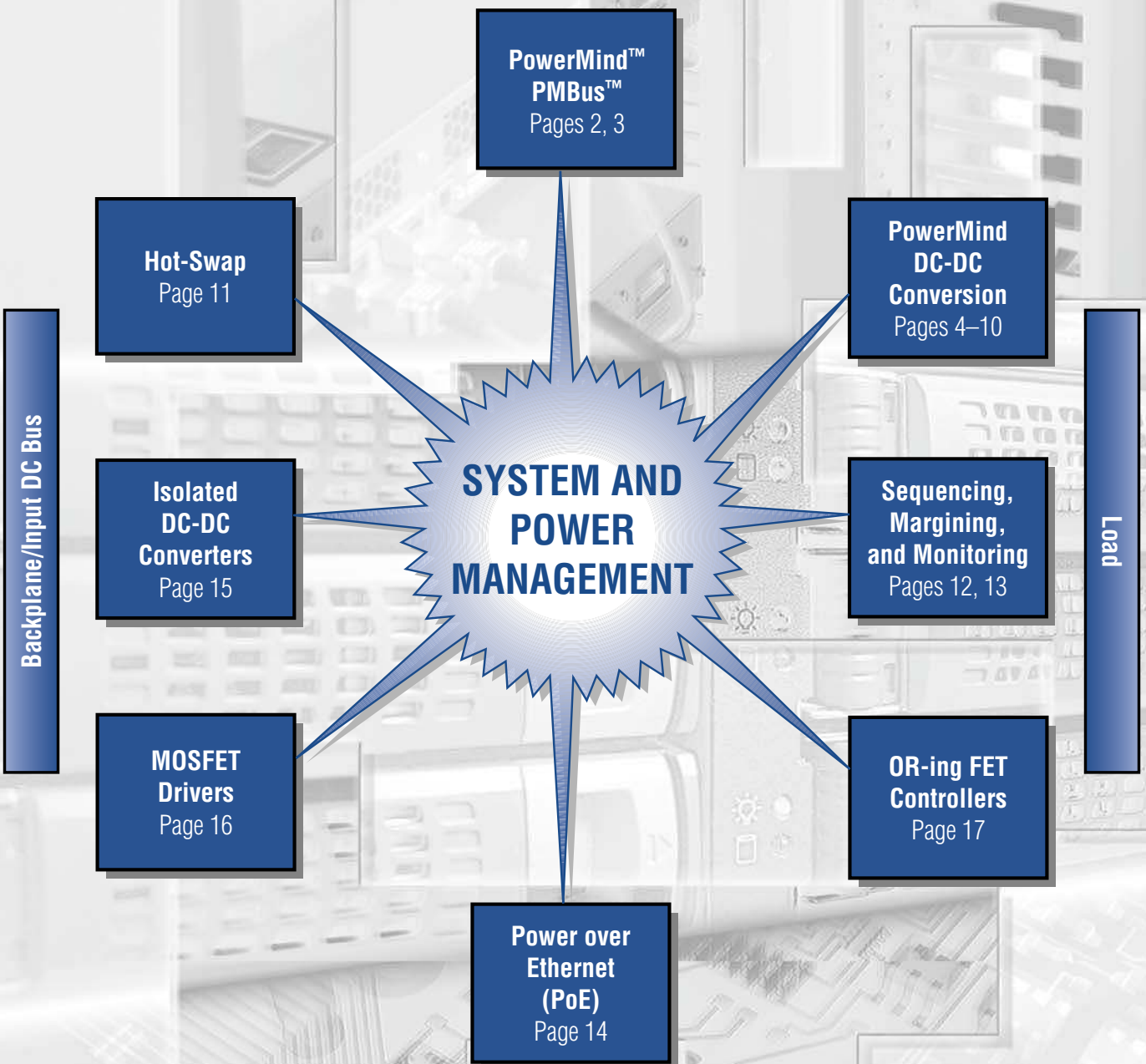

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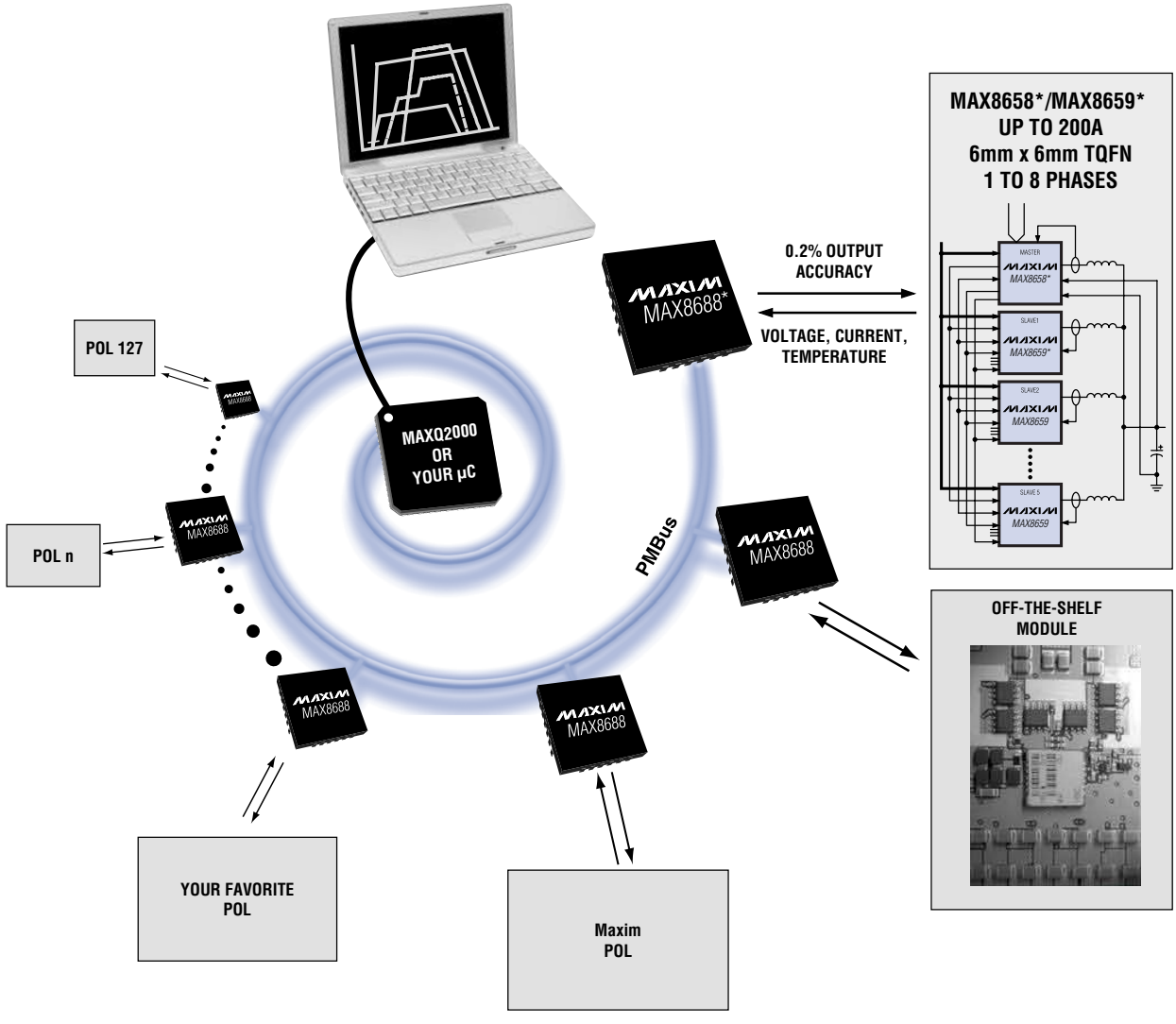

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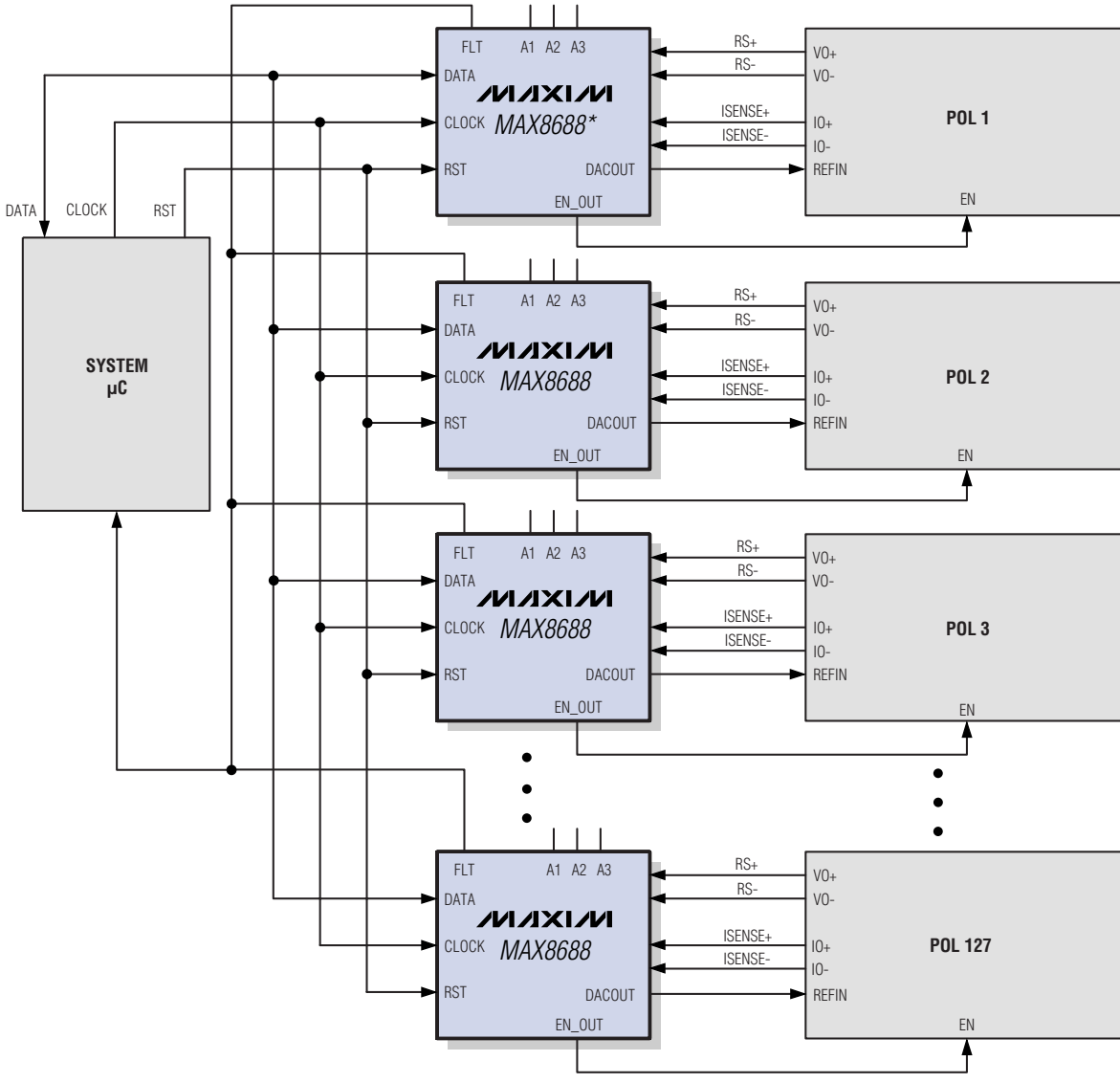

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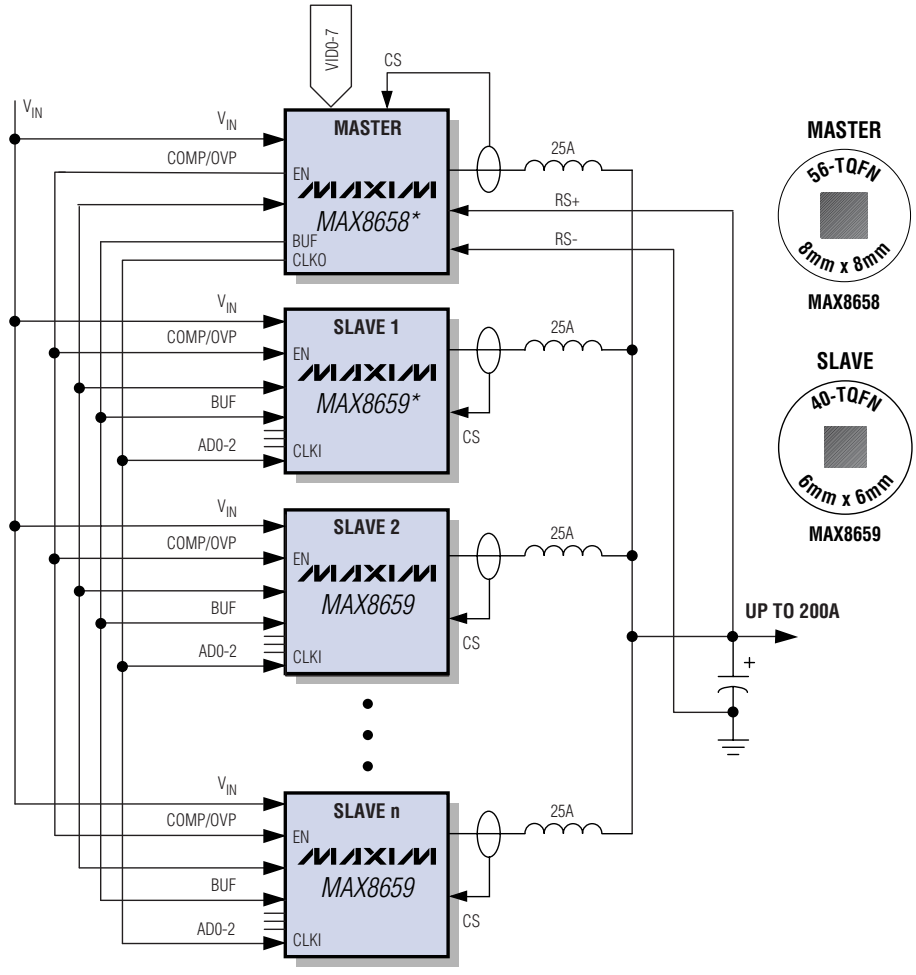

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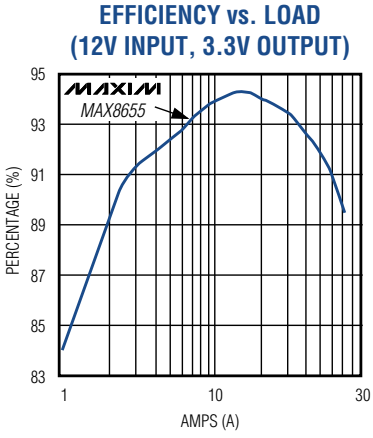

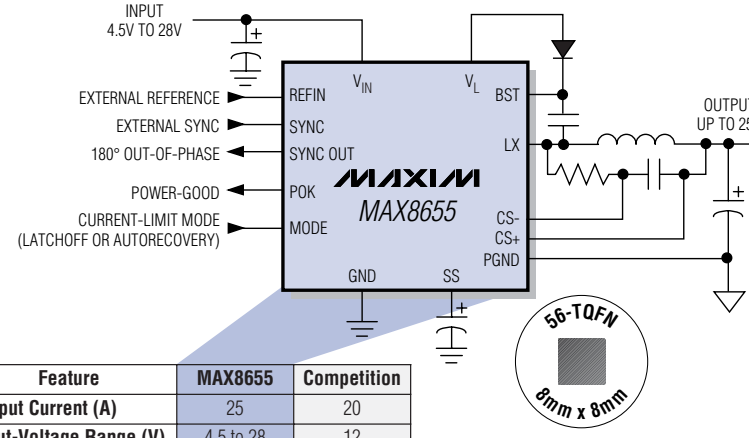

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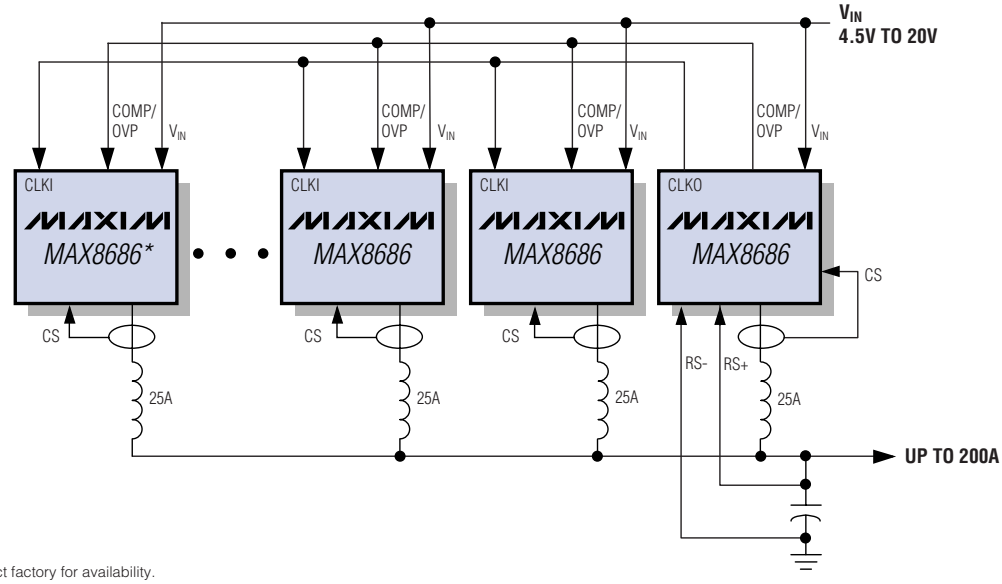

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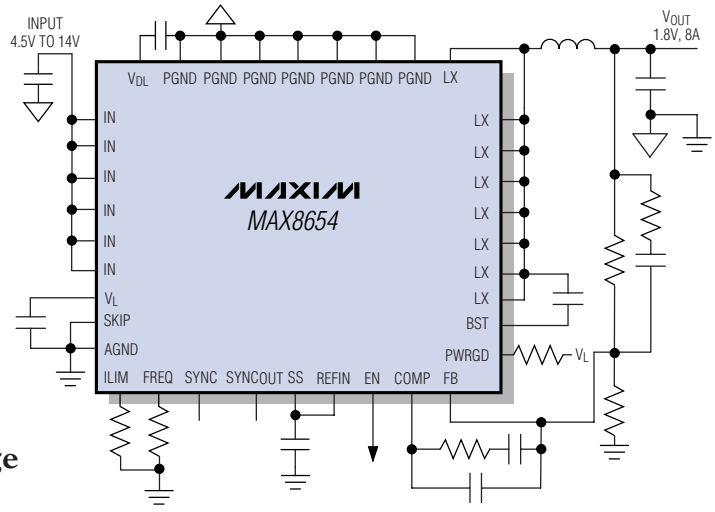

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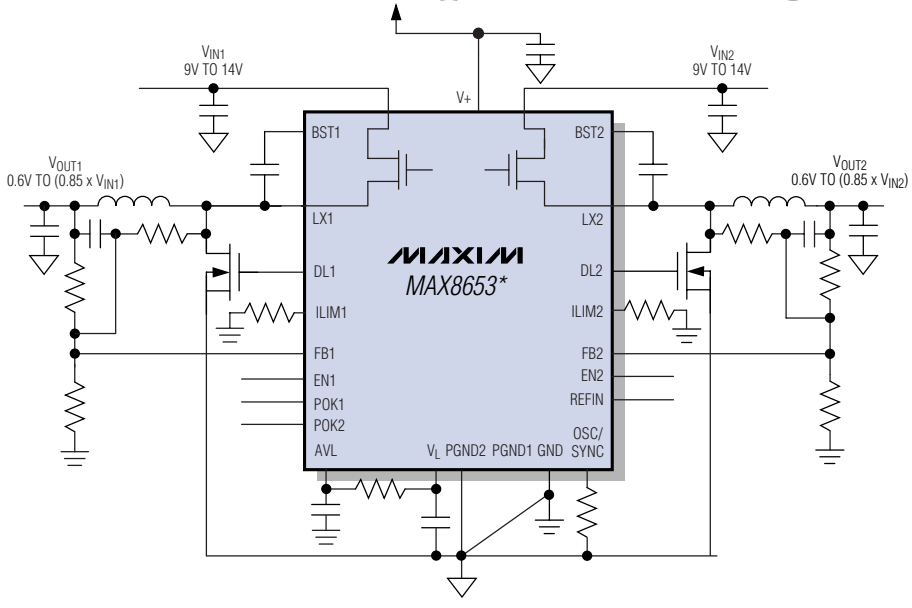

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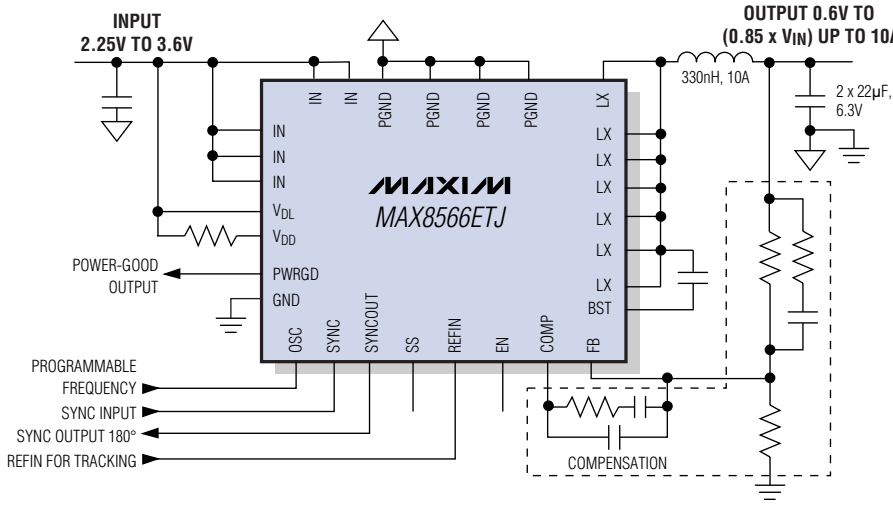

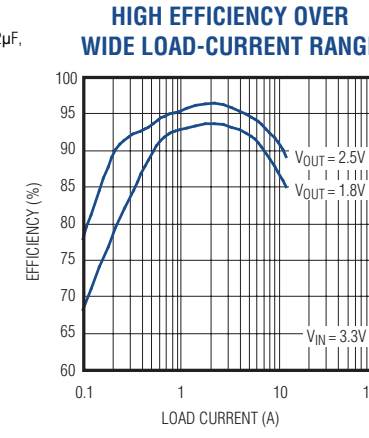

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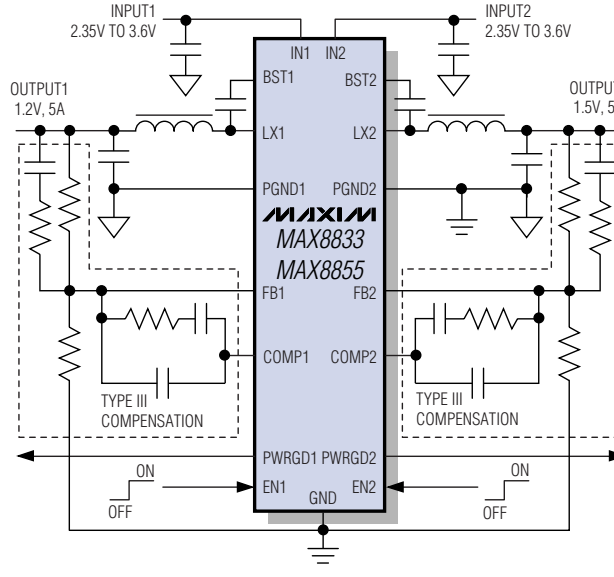
- DDR Termination
- Memory, Telecom/Datacom, and POL Power Supplies

Dual 3A/Dual 5A, 2MHz Step-Down Regulators with Integrated MOSFETs

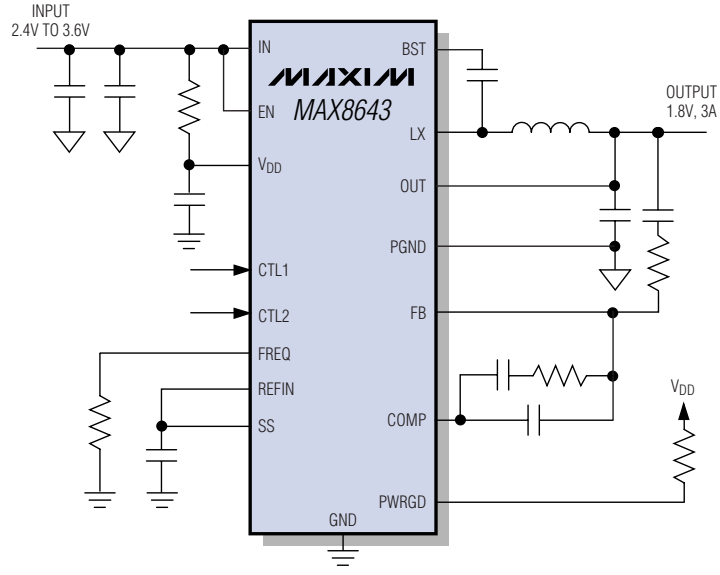
- Dual 3A (MAX8833) or Dual 5A (MAX8855) Outputs
- 0.5MHz to 2MHz Adjustable Switching or FSYNC Input
- All-Ceramic Capacitor Design
- 180° Out-of-Phase Operation Reduces Input Inrush Current
- Individual Enable Inputs and POK Outputs
- 5mm x 5mm, 32-Pin TQFN Package



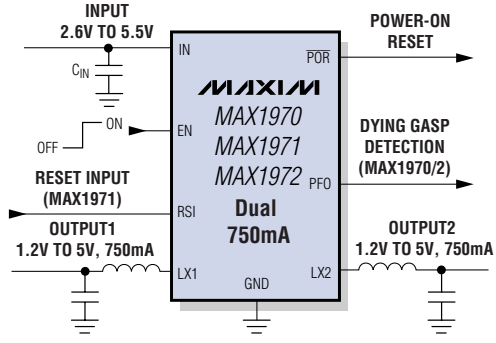
PowerMind DC-DC Conversion

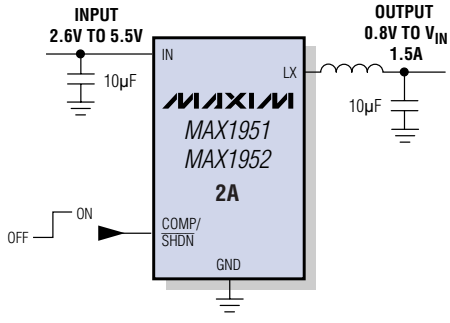
2.35V to 3.6V Input, 3A/6A Internal Switch, Step-Down PWM Buck Regulators

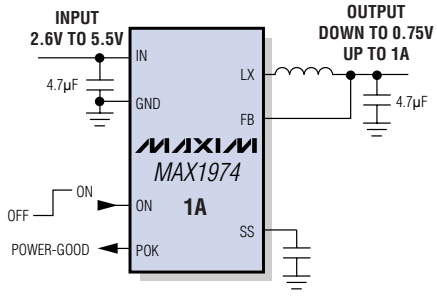
- 38mΩ/27mΩ On-Resistance MOSFETs
- ±1% Output Accuracy over Load and Line
- 500kHz to 2MHz Adjustable Switching
- Adjustable Output from 0.6V to (0.85 x V_{IN})
- VID-Set Output Voltages (0.6, 0.7, 0.8, 1.0, 1.2, 1.5, 1.8, 2.0, and 2.5V)
- 4mm x 4mm, 24-Pin TQFN Package

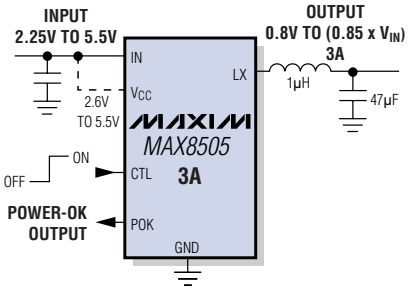


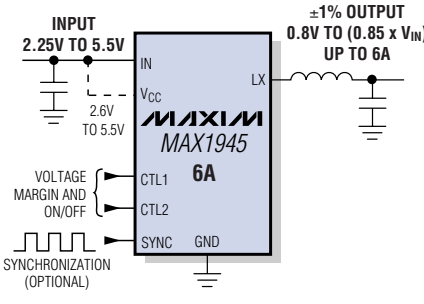
5V, Internal Switch, Step-Down Regulators





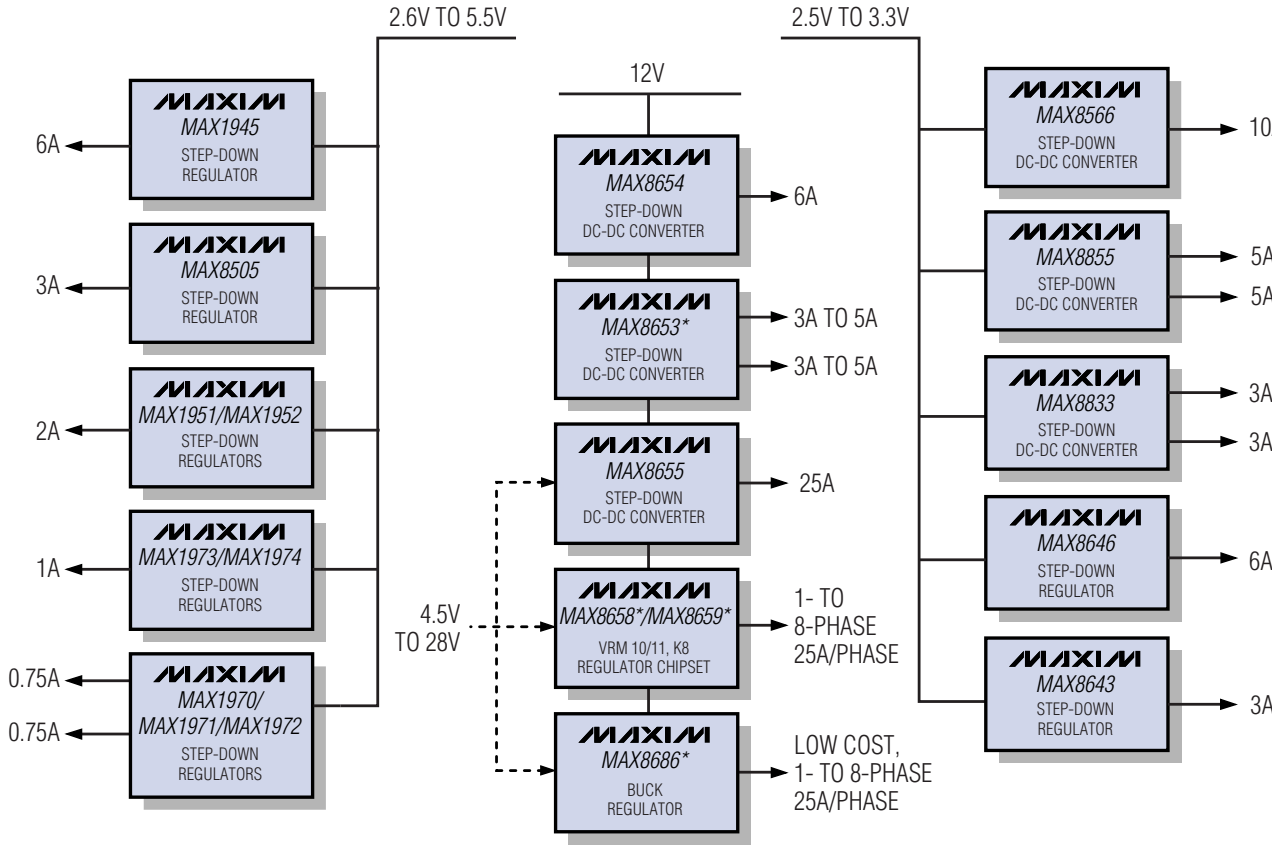






Maxim's Complete Selection of PowerMind Products for Your Power-Supply Designs

PowerMind DC-DC Conversion



For a Complete Selection of Maxim's DC-DC Converters, See Pages 18 and 19

Inductor Choice Yields Performance Tradeoffs in DC-DC Converters

Cost, size, resistance, and current capability drive the choice of inductor for most step-down DC-DC switching converters. Many such applications specify the inductor value shown in the switching converter's data sheet or evaluation kit, but those values are usually specific to application or performance criteria. Portable applications, for instance, uphold size as the main consideration because such little space is available. This application note evaluates inductors for efficiency, noise (output ripple), and transient response using an evaluation kit designed for the MAX8646 step-down regulator.

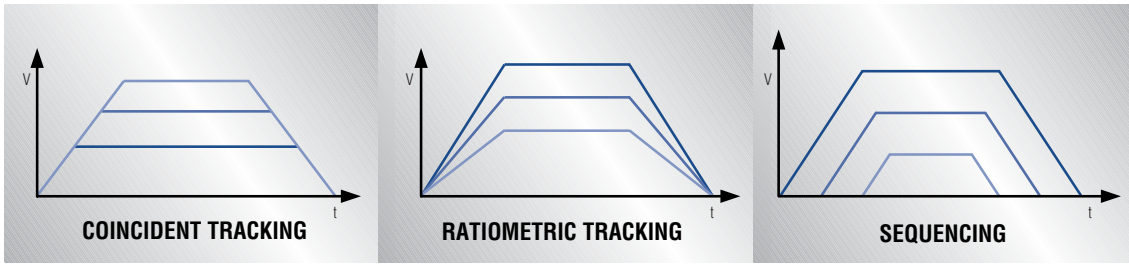
For the complete application note, go to: www.maxim-ic.com/AN3988

*Future product—contact factory for availability.

DC-DC Conversion

High-Performance, Multiphase, Triple Step-Down Controller Has Sequencing and Tracking Control

Flexible Controller Delivers Up to 15A per Output



High Integration

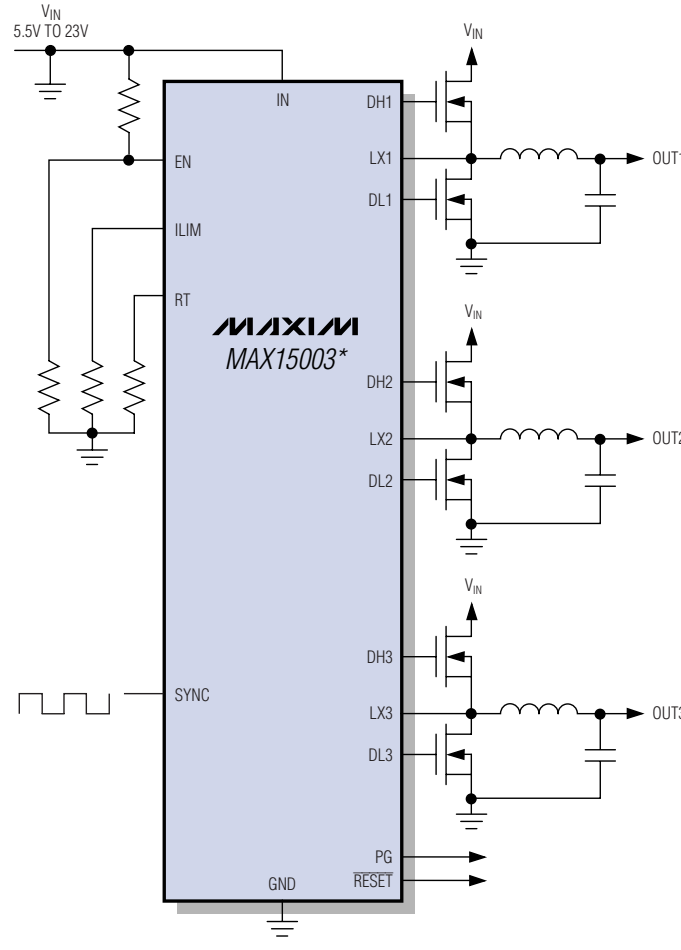
- Triple Synchronous Step-Down Controller in a Single Package
- Reset and Independent Power-Good Outputs
- Hiccup Current, Current Sense, and Thermal Shutdown Protection

High Performance

- High-Current Drivers Deliver 15A per Output
- 120° Out-of-Phase Operation Reduces Input Ripple Current and Input Capacitance
- ±1% Accurate Internal Reference
- High Switching Frequencies (Up to 2.2MHz) Minimize Passive Components

Flexibility

- Adjustable Output Voltage, Current Limit, Compensation, and Switching Frequency for Optimizing Design
- External SYNC Input for External Clock Signal



EV KIT AVAILABLE

Part	Configuration	Package (mm x mm)
MAX15002*	Dual	40-TQFN (6 x 6)
MAX15003*	Triple	48-TQFN (7 x 7)

*Future product—contact factory for availability.

Industry's Most Robust and Versatile Hot-Swap Controllers

Superior Fault Protection; Lowest Current-Sense Threshold; Hot-Swap Voltage Rails Down to 1V or Up to 80V

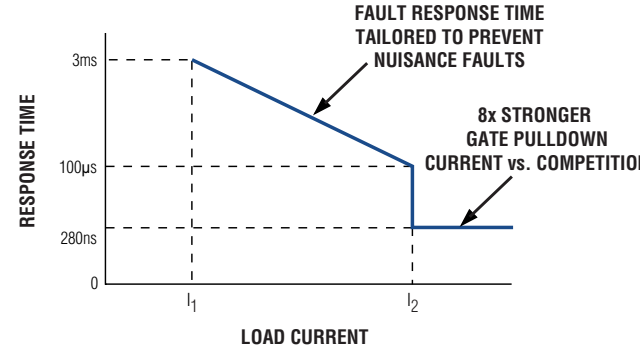
ADVANTAGES OVER THE COMPETITION

MOST VERSATILE

(MAX5902/03/24/25)

MOST ROBUST

(MAX5924/25/39)



SMALLEST

MAXIM

MAX5902/MAX5903

3mm x 3mm
SOT23 vs. Competition's
4mm x 5mm QFN

LOWEST CS THRESHOLD

MAXIM

MAX5925

10mV Current-Sense
Threshold, 5x Lower
than Competition

FAST

MAXIM

MAX5939

Turns Off
MOSFET in < 280ns

LOW VOLTAGE

MAXIM

MAX5924

Hot-Swaps Voltage
Rails Down to 1V

HIGH VOLTAGE

MAXIM

MAX5933

Hot-Swaps Voltage
Rails Up to 80V

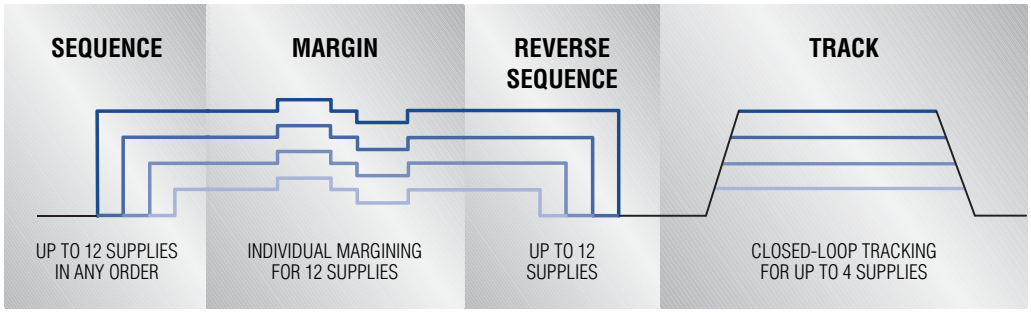
Sample Our Hot-Swap Controllers:
www.maxim-ic.com/HotSwap-info

Sequencing, Margining, Monitoring

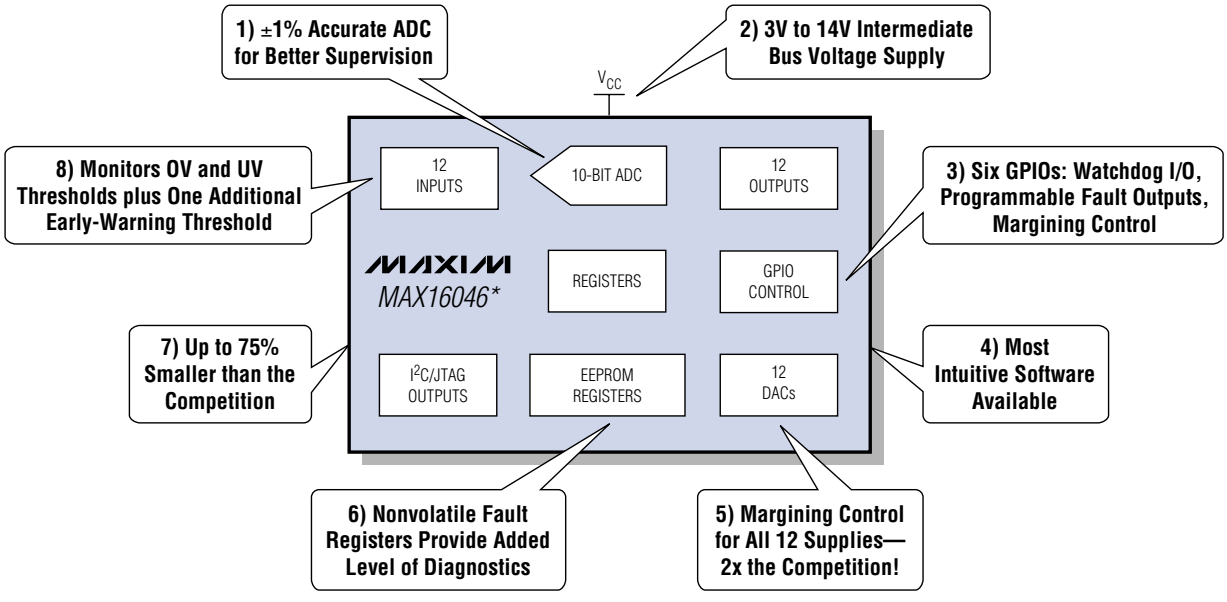
Most Integrated Fault-Monitoring, Sequencing, and Margining IC

FUTURE PRODUCTS

NV Fault Registers Store 12 Channels of Data on System Failure



EIGHT ADVANTAGES OVER THE COMPETITION

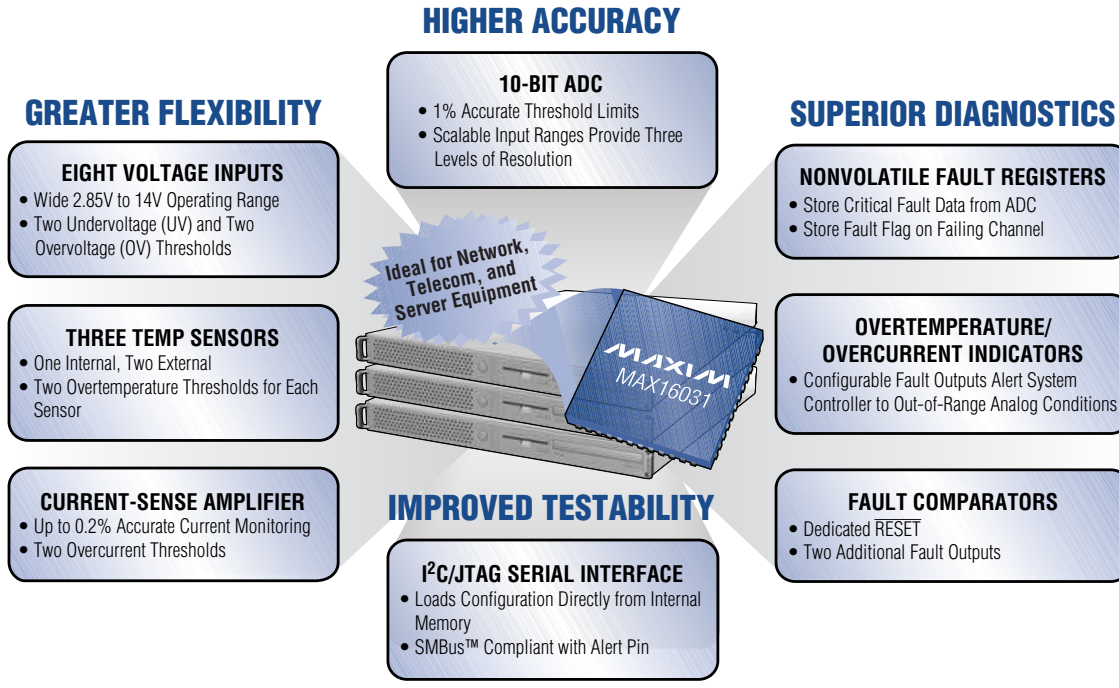


Part	No. of Voltages Monitored	No. of Outputs/FET Drivers	Reverse Sequencing	Supply Adjustment/ Margining	ADC for Voltage Readback	No. of Voltages Tracked	OV Monitoring	Operates Off of Intermediate Bus Voltage	No. of GPIOs	Package (mm x mm)
MAX16046*	12	12/6	✓	12 DACs	✓	4	✓	✓	6	56-TQFN (8 x 8)
MAX16047*	12	12/6		—						
MAX16048*	8	8/6		8 DACs						
MAX16049*	8	8/6		—						

*Future product—contact factory for availability.

System Monitor ICs Ensure Highest Reliability

Nonvolatile Fault Registers Store Voltage, Temperature, and Current Measurements to EEPROM



MAX16031/MAX16032* Advantages over the Competition

- Higher Resolution ADC Provides Greater Accuracy
- Nonvolatile Fault Registers Assist with Debugging and Failure Analysis
- EEPROM-Configurable Thresholds Maximize Design Flexibility
- Additional Temp Sensors Protect Critical System Components
- Current Monitoring Protects System from Damaging Current Spikes
- Wide Operating Range Allows System to Operate from an Intermediate Bus Voltage
- Three Configurable Fault Outputs Notify System Controller of Out-of-Range Analog Conditions

Part	No. of Voltage Inputs		RESET Output	OV and UV Monitoring	ADC	Temperature Sensor	Current Sensor	No. of Fault Outputs	No. of GPIOs	Package
	Single-Ended	Differential								
MAX16031	8	4	✓	✓	✓	1 int, 2 ext	✓	4	2	48-TQFN
MAX16032*	6	3				1 int, 1 ext				

SMBus is a trademark of Intel Corporation.
*Future product—contact factory for availability.

PoE

Highly Integrated, End-to-End PoE Solutions for PSEs and PDs

Meet IEEE 802.3af Specifications and Enable High-Power (PoE+) Applications

Power-Sourcing Equipment (PSE)

High Power (MAX5952 Quad PSE Controller)

- Exceeds 15W IEEE 802.3af Limit
- Delivers Up to 45W per Port

Superior Design Flexibility (MAX5945/52 Quad PSE Controllers)

- Manual, Semiautomatic, and Automatic Modes Ease System Debug and Field Diagnostics

Single-Port/Multiport PSE Reference Designs

- 15W to 70W Single Port or Multiport
- Midspan and Endpoint Applications

Powered Devices (PDs)

Superior Design Flexibility (MAX5941/42 IEEE 802.3af-Compliant PD Interface with PWM Controller)

- Programmable Inrush Current
- Single-Chip Solution Replaces Two ICs

Support Legacy PSEs (MAX5940 IEEE 802.3af-Compliant PD Interface Controller)

- Adjustable UVLO Allows Operation with Legacy PSE Systems

30W Isolated/Nonisolated Reference Designs

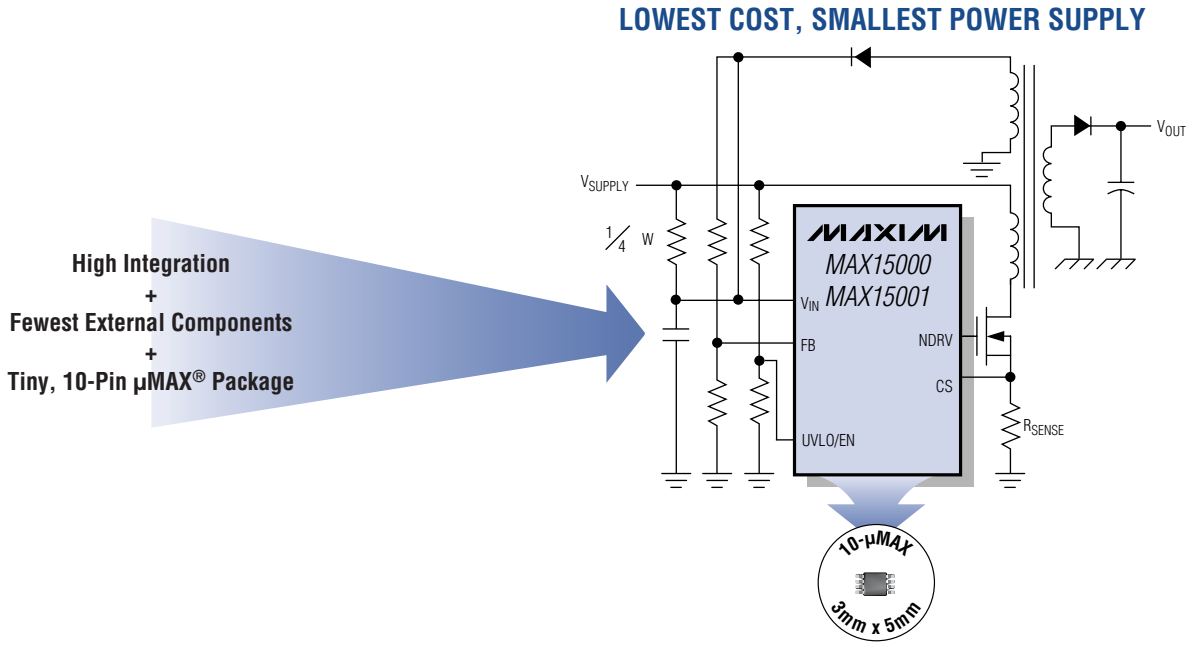
- Bypass Internal PD MOSFET for PoE+ Applications

For More Information and to Request Reference Designs, Go to: www.maxim-ic.com/PoE

Smallest, Low-Cost PWM Controllers Support Universal Offline, Telecom, and 12V Input Voltages

Isolated DC-DC Conversion

Internal Error Amplifier Allows Isolated or Nonisolated Designs



High Integration/High Performance

- 50µA Startup Current Means High Efficiency in Standby Mode
- Soft-Start Eliminates Output-Voltage Overshoot and Guarantees Monotonic Rise During Power-Up
- 1A Gate-Drive Current

Design Flexibility/High Reliability

- Externally Programmable Startup Voltage Prevents Brownout Conditions
- Remote ON/OFF
- Thermal Shutdown

Saves Space

- 10-Pin µMAX Package Is 50% Smaller than Competitor's 8-Pin SO
- 12.5kHz to 625kHz (adj) Switching Frequency Optimizes Power Magnetics and Eases Filtering

Reduces Power-Supply Cost

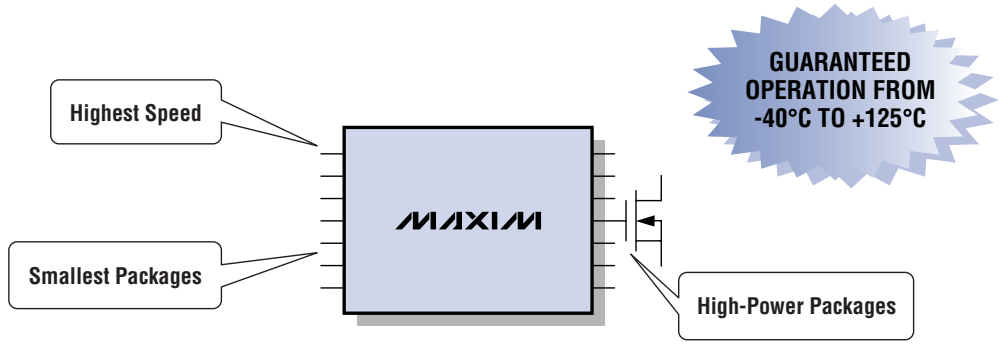
- Internal Error Amplifier for Primary-Side Regulation Eliminates Cost of Optocoupler and Shunt Reference in Isolated Power Supplies
- Internal 24V Regulator Simplifies Controller-Biasing Design, Provides Consistent and Safe Gate-Drive Voltage

To See a Wide Selection of PWM Controllers for Isolated Power Supplies, Go to: www.maxim-ic.com/PowerSupplies

MOSFET Drivers

Highest Speed and Smallest Size MOSFET Drivers

Up to 52% Lower Propagation Delay and 44% Smaller Footprint than Nearest Competitor; Available in Thermally Enhanced High-Power Packages



Highest Speed for High-Frequency, Compact Power Supplies

- As Low as 12ns Prop Delay (MAX5048)—52% Lower than Competition
- Guaranteed Prop-Delay Matching from Part to Part (MAX5078)—Not Available from Competition

Smallest Packages for Compact 1/8th and 1/16th Brick Modules

- 4A Drivers in Tiny, 3mm x 3mm, 8-Pin TDFN (MAX5054)—44% Smaller than 10-Pin LLP Package
- 7.6A Driver in Tiny, 3mm x 3mm, 6-Pin SOT23 (MAX5048)—56% Smaller than TSSOP

High-Power Packages

- Exposed-Pad Package Keeps Die Less than +10°C Above PCB Temperature
- Up to 1.45W Dissipation at +70°C Ambient Temperature

Part	Description	Input Voltage (V, max)	Peak Source/Sink Current (A)	Prop Delay (ns)	Package
MAX5048	Low-side MOSFET driver	V_{DD} = 12.6	1.3/7.6	12	6-SOT23/TDFN
MAX5054/MAX5078	Low-side MOSFET driver	V_{DD} = 15	4/4	20	6-TDFN, 8-TDFN
MAX5062/MAX5063/ MAX5064	High-speed, half-bridge MOSFET driver	125	2/2	35	8-SO-EP, 12-TQFN
MAX15018*/MAX15019*	High-speed, half-bridge MOSFET driver	125	3/3	35	8-SO-EP
MAX15024*/MAX15025*	Low-side, single/dual MOSFET driver	V_{DD} = 28	8/4	16	10-TDFN

www.maxim-ic.com/MOSFET

*Future product—contact factory for availability.

OR-ing MOSFET Controller Has Fastest (200ns) MOSFET Turn-Off and Best Fault Tolerance

The MAX5079 replaces OR-ing diodes with low-voltage-drop MOSFETs in high-current, parallel, redundant power supplies. The MAX5079 is ideal for servers, RAID storage, networking switch/routers, and silver boxes.

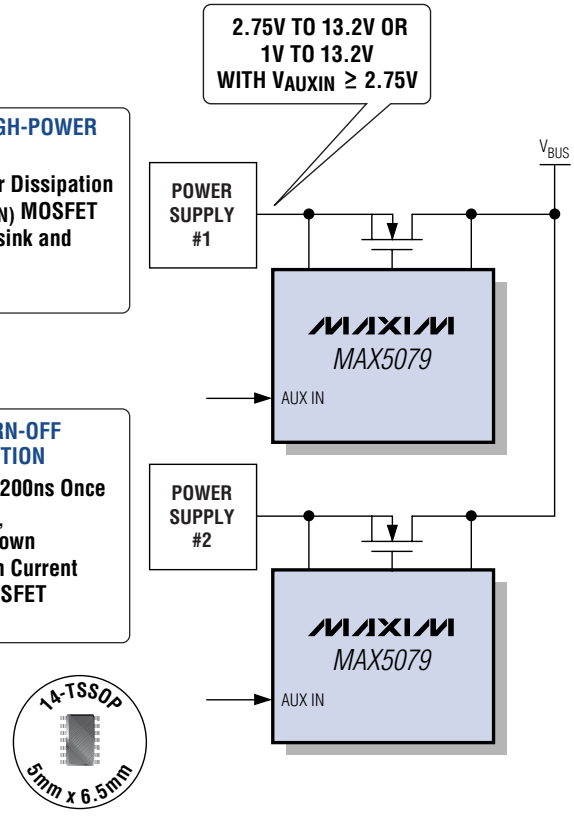
FOUR REASONS WHY THE MAX5079 IS YOUR BEST CHOICE

1 REPLACES BULKY, HIGH-POWER DISSIPATION DIODES

- Eliminates High-Power Dissipation Diode with Low $R_{DS(ON)}$ MOSFET
- Eliminates Bulky Heatsink and Reduces Size
- Reduces Cost

2 FASTEST MOSFET TURN-OFF DURING FAULT CONDITION

- Turns Off in Less than 200ns Once V_{IN} Drops Below V_{BUS}, Preventing V_{BUS} Pulldown
- High 3A Gate Pulldown Current Ensures Ultra-Fast MOSFET Turn-Off



3 HIGHEST LEVEL OF FAULT TOLERANCE

- Turns Off MOSFET When $V_{IN} < V_{BUS}$
- Continues to Control MOSFET by Taking Power from V_{BUS} or Auxiliary Power Supply When V_{IN} Fails
- Detects and Reports Supply UV and Bus OV

4 HIGH FLEXIBILITY ALLOWS DESIGN OPTIMIZATION

- Adjustable MOSFET Reverse-Voltage Threshold Eliminates Nuisance Trips Due to Glitches at V_{BUS}
- Additional Slow Comparator with Adjustable Threshold and Blanking Time Eliminates Nuisance Trips During Hot-Plugging

Additional OR-ing Controllers

Part	Bus Voltage (V)	Description	Package
MAX5079	12	Provides high flexibility and protection features	14-TSSOP
MAX5943	12	Single controller for FireWire® applications (limiter + OR-ing)	16-QSOP
MAX5944	12	Dual controller for FireWire applications (limiter + OR-ing)	16-SO
MAX8535/MAX8585	12	Simple, low-cost solution for 12V	8-µMAX
MAX8536	3.3 or 5	Controller for low-voltage applications	8-µMAX

FireWire is a registered trademark of Apple, Inc.

Internal Switch DC-DC Converters

Part	$V_{IN, MIN}$ (V)	$V_{IN, MAX}$ (V)	$I_{OUT, MAX}$ (A)	$V_{OUT, MAX}$ (V)	$V_{OUT, MAX}$ (V)	Topology Mode	Enable	Power-Good	External Sync	Clock-Out Signal	Voltage Margining	Package (mm x mm)	Key Features	Desktop PC	Notebook	Server	Graphics Card	Printer	Storage	Telecom
Single-Output Step-Down																				
MAX1945	2.6	5.5	6	0.8	0.85 x V_{IN}	Current	✓		✓	✓	✓	20-TSSOP-EP	500kHz or 1MHz operation, built-in margining			✓	✓		✓	✓
MAX1973	2.6	5.5	1	1.25	V_{IN}	Current					✓	10-µMAX	Margining, selectable preset outputs		✓	✓		✓	✓	✓
MAX1974	2.6	5.5	1	0.75	V_{IN}	Current	✓	✓				10-µMAX	Selectable preset outputs	✓	✓	✓		✓	✓	✓
MAX1951	2.6	5.5	2	0.8	V_{IN}	Current						8-SO	Available reference as an output	✓	✓	✓		✓	✓	✓
MAX1952	2.6	5.5	2	1.8	V_{IN}	Current	✓		✓	✓	✓	8-SO	Available reference as an output		✓	✓		✓	✓	✓
MAX8643/46	2.3	3.6	3/6	0.5	0.85 x V_{IN}	Voltage	✓	✓	✓	✓		TQFN (4 x 4)	Up to 2MHz, very efficient, 9 preset outputs			✓			✓	✓
MAX8505	2.6	5.5	3	0.8	0.85 x V_{IN}	Current	✓	✓	✓	✓	✓	16-QSOP	500kHz or 1MHz operation		✓	✓		✓	✓	✓
MAX8566	2.3	3.6	10	0.5	0.85 x V_{IN}	Voltage	✓	✓	✓	✓		32-TQFN (5 x 5)	Up to 2MHz, very efficient			✓			✓	✓
MAX8654	4.5	14	8	0.5	0.85 x V_{IN}	Voltage	✓	✓	✓	✓		TQFN (6 x 6)	Up to 1MHz			✓			✓	✓
MAX8655	4.5	28	25	0.7	0.9 x V_{IN}	Current	✓	✓	✓	✓		TQFN (8 x 8)	Up to 1MHz with full protection			✓	✓		✓	✓
Dual-Output Step-Down																				
MAX1970/72	2.6	5.5	25	0.8	8	Current	✓	✓	✓			16-QSOP	POR, power-fail output		✓	✓		✓	✓	✓
MAX1971	2.6	5.5	25	0.8	8	Current	✓	✓	✓			16-QSOP	POR, PSI		✓	✓		✓	✓	✓
MAX8833/55	2.35	3.6	2 x 3A	0.6	0.9 x V_{IN}	Voltage	✓					TQFN (5 x 5)	Dual outputs with 180° out-of-phase operation		✓	✓		✓	✓	✓

Nonisolated DC-DC Converters

Part	$V_{IN, MIN}$ (V)	$V_{IN, MAX}$ (V)	$I_{OUT, MAX}$ (A)	$V_{OUT, MIN}$ (V)	$V_{OUT, MAX}$ (V)	Topology Mode	Enable	Power-Good or Reset	External Sync	Clock-Out Signal	Package (mm x mm)	Key Features	Desktop PC	Notebook	Server	Graphics Card	Printer	Storage	Telecom Power	Network Power	Base Station	Cable and xDSL Modem	Router	Set-Top Box	VoIP Supply	SLIC Supply	Industrial Power Supply	Automotive Power Supply
Single-Phase, Step-Down Switchers																												
MAX1953	3	5.5	10	0.8	0.86 x V_{IN}	Current					10-µMAX	Adjustable current limit, 1MHz, all ceramic, smallest footprint solution				✓	✓	✓	✓	✓	✓		✓	✓	✓				
MAX1954	3	13.2	10	0.8	0.86 x V_{IN}	Current					10-µMAX	300kHz, 3V to 13.2V input range, 25A capability	✓	✓		✓	✓	✓	✓	✓			✓	✓					
MAX1954(A)	3	13.2	10	0.8	0.86 x V_{IN}	Current					10-µMAX	300kHz, 3V to 13.2V input range, 25A capability, foldback current limit	✓	✓		✓	✓	✓	✓	✓			✓	✓					
MAX1960/61	2.35	5.5	20	0.8	0.86 x V_{IN} / 0.90 x V_{IN}	Voltage	✓		✓	✓	20-QSOP	500kHz or 1MHz, or external sync up to 1.2MHz; on-board charge pump generates regulated 5V gate drive; clock output; ±4% voltage-margining controls; $R_{DS(ON)}$ current sense; adjustable output voltage (MAX1960) or 4 preset output voltages (MAX1961)			✓			✓	✓									
MAX1962	2.35	5.5	20	0.8	0.90 x V_{IN}	Voltage	✓		✓	✓	20-QSOP	500kHz or 1MHz, or external sync up to 1.2MHz; on-board charge pump generates regulated 5V gate drive; clock output; ±4% voltage-margining controls; ±10% accurate resistor current sense; adjustable or 4 preset output voltages			✓			✓	✓									
MAX1966	2.7	5.5	10	0.8	0.90 x V_{IN}	Voltage					8-SO	Single-input supply, 100kHz				✓			✓	✓		✓	✓	✓				✓
MAX1967	2.7	28	10	0.8	0.90 x V_{IN}	Voltage					10-µMAX	Wide input range, single-input supply, 100kHz				✓			✓	✓		✓	✓	✓				✓
MAX8543	3	13.2	25	0.8	0.90 x V_{IN}	Current	✓		✓		16-QSOP	200kHz to 1MHz, ±1% accuracy, prebias startup, autorecovery current limit						✓	✓	✓	✓							
MAX8544	3	13.2	25	0.8	0.90 x V_{IN}	Current	✓	✓	✓	✓	20-QSOP	200kHz to 1MHz, ±1% accuracy, prebias startup, autorecovery current limit or latchoff, CLKOUT signal						✓	✓	✓	✓							
MAX8545/46	2.7	28	10	0.8	0.9 x V_{IN}	Voltage					10-µMAX	Wide input range, single-input supply, 300kHz, foldback current limit	✓	✓		✓	✓	✓	✓	✓		✓	✓	✓				
MAX8548	2.7	28	10	0.8	0.9 x V_{IN}	Voltage					10-µMAX	Wide input range, single-input supply, 100kHz, foldback current limit	✓	✓		✓	✓	✓	✓	✓		✓	✓	✓				
MAX8576	3	28	10	0.6	0.9 x V_{IN}	Hysteretic					10-µMAX	200kHz to 500kHz, no compensation, on-board LDO, prebias startup, OVP	✓	✓		✓	✓											

Nonisolated DC-DC Converters (cont.)

Part	$V_{IN, MIN}$ (V)	$V_{IN, MAX}$ (V)	$I_{OUT, MAX}$ (A)	$V_{OUT, MIN}$ (V)	$V_{OUT, MAX}$ (V)	Topology Mode	Enable	Power-Good or Reset	External Sync	Clock-Out Signal	Package (mm x mm)	Key Features	Desktop PC	Notebook	Server	Graphics Card	Printer	Storage	Telecom Power	Network Power	Base Station	Cable and xDSL Modem	Router	Set-Top Box	VoIP Supply	SLIC Supply	Industrial Power Supply	Automotive Power Supply
MAX8577	3	28	10	0.6	0.90 x V_{IN}	Hysteretic					10-µMAX	200kHz to 500kHz, no compensation, on-board LDO, OVP	✓	✓		✓	✓												
MAX8578	3	28	10	0.6	0.90 x V_{IN}	Hysteretic	✓				10-µMAX	200kHz to 500kHz, no compensation, prebias startup, OVP	✓	✓		✓	✓												
MAX8579	3	28	10	0.6	0.90 x V_{IN}	Hysteretic	✓				10-µMAX	200kHz to 500kHz, no compensation, OVP	✓	✓		✓	✓												
MAX8597	4.5	28	25	0.6	0.995 x V_{IN}	Voltage	✓	✓			20-TQFN (4 x 4)	Low dropout with all n-channel MOSFETs, 200kHz to 1.4MHz, prebias startup, EN and POK, uncommitted op amp for fan control/remote sense		✓	✓			✓	✓										
MAX8598/99	4.5	28	25	0.6	0.995 x V_{IN}	Voltage	✓	✓			16-TQFN (4 x 4)	Low dropout with all n-channel MOSFETs, 200kHz to 1.4MHz, prebias startup, EN and POK, OVP (MAX8599)		✓	✓			✓	✓										
Dual-Phase Switchers																												
MAX1858	4.75	23	10	0.4	0.8 x V_{IN}	Voltage	✓	✓	✓	✓	24-QSOP	Voltage sequencing, 100kHz to 600kHz, out-of-phase dual step-down, foldback current limit, POR	✓	✓	✓	✓		✓	✓	✓		✓	✓	✓				
MAX1875	4.75	23	10	0.4	0.8 x V_{IN}	Voltage	✓		✓	✓	24-QSOP	Voltage sequencing, 100kHz to 600kHz, out-of-phase dual step-down, foldback current limit			✓	✓		✓	✓	✓		✓	✓	✓				
MAX1876	4.75	23	10	0.4	0.8 x V_{IN}	Voltage	✓	✓	✓	✓	24-QSOP	Voltage sequencing, 100kHz to 600kHz, out-of-phase dual step-down, foldback current limit, POR			✓	✓		✓	✓	✓		✓	✓	✓				
MAX1955/56	2.25/ 1.6	5.5	25	0.8	0.90 x V_{IN}	Voltage	✓		✓		28-TQFN (5 x 5)	Voltage sequencing, 600kHz or external sync, out-of-phase dual step-down, voltage margining, foldback current limit			✓			✓	✓	✓								
MAX5066	4.5	28	50	0.8	0.90 x V_{IN}	Average current	✓	✓	✓		28-TQFN (5 x 5)	Dual single-phase output or single dual-phase for high-current output			✓	✓		✓	✓	✓	✓	✓	✓				✓	✓
MAX8529	4.75	23	25	0	18	Voltage	✓	✓	✓	✓	28-TSSOP-EP	Voltage sequencing, 600kHz to 1.5MHz, out-of-phase dual step-down, foldback current limit, POR			✓	✓		✓	✓	✓		✓	✓	✓				✓
Complete DDR Solutions																												
MAX8537	4.5	23	25	0.8	3.6	Voltage	✓	✓			28-QSOP	Complete DDR solution including V_{DDQ} (PWM), V_{TT} (PWM), and V_{TTR}; 200kHz to 1.4MHz, ±1% accuracy, supports all-ceramic decoupling	✓	✓	✓	✓		✓		✓		✓	✓					
MAX8550(A)/ MAX8632	2	28	15	0.7	5.5	Quick-PWM™	✓	✓			28-TQFN (5 x 5)	Complete DDR solution including V_{DDQ} (PWM), V_{TT} (3A LDO), and V_{TTR}	✓	✓	✓	✓		✓		✓								
MAX8551	2	28	15	0.7	5.5	Quick-PWM	✓	✓			28-TQFN (5 x 5)	Complete DDR solution including V_{DDQ} (PWM), V_{TT} (3A LDO), and V_{TTR}	✓		✓	✓		✓		✓								
DDR V_{TT} Solutions																												
MAX1957	3	5.5	3	0.4	0.8 x V_{IN}	Current					10-µMAX	300kHz, small footprint, low cost	✓		✓	✓	✓	✓	✓	✓			✓	✓				
MAX1917	1.5	14	25	0.4	0.8 x V_{IN}	Quick-PWM					16-QSOP	Fastest response minimizes output caps, 200kHz/300kHz/400kHz/550kHz preset switching frequencies, ±1% accuracy	✓	✓	✓			✓		✓								
MAX8553	1.5	22	25	0.4	0.8 x V_{IN}	Quick-PWM					16-QSOP	Pin compatible with MAX1917, OVP, wide input range	✓	✓	✓			✓		✓								
Boost Regulators																												
MAX1708/09	1	5.5	3.5/ 6	2.5	5.5	Current	✓		✓		16-QSOP/ 16-SO (narrow)	Integrated 5A/10A MOSFET switch, 600kHz or synchronizable up to 1MHz, fixed 3.3V and 5V outputs or adjustable			✓				✓	✓			✓	✓				✓
Inverting Regulators																												
MAX1846	3	16.5	10	-100m	-200	Current					10-µMAX	100kHz to 500kHz, electrolytic or ceramic output capacitors, negative voltages up to -200V			✓				✓	✓	✓					✓	✓	✓
MAX1847	3	16.5	10	-100m	-200	Current	✓		✓		16-QSOP	100kHz to 500kHz, electrolytic or ceramic output capacitors, negative voltages up to -200V, flyback capability with n-channel MOSFET			✓				✓	✓	✓					✓	✓	✓
MAX1856	3	28	10	-100m	-200	Current	✓		✓		10-µMAX	Flyback inverter using low-cost transformer, 100kHz to 500kHz Idle Mode™ improves light load efficiency										✓	✓	✓	✓	✓	✓	

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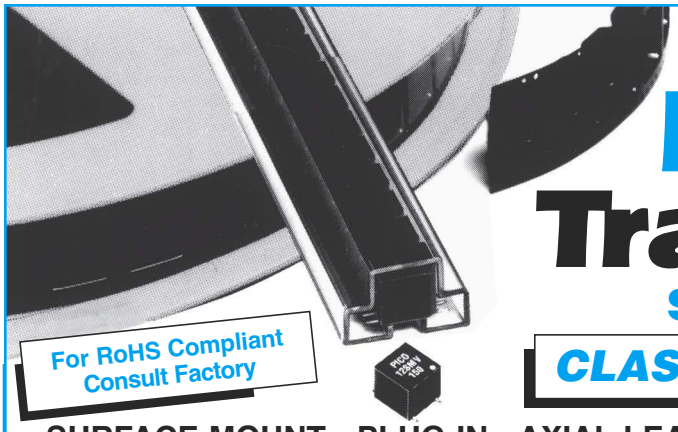

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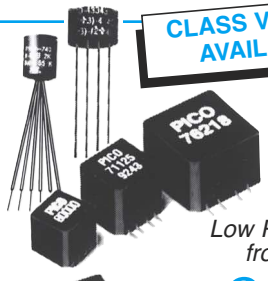

CLASS V (155°C) AVAILABLE

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Surface Mount

All PICO surface mount units utilize materials and methods to withstand extreme temperatures of reflow procedures without degradation of electrical or mechanical characteristics.

AUDIO TRANSFORMERS

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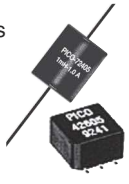

PULSE TRANSFORMERS

10 Nanoseconds to 100 Microseconds. ET Rating to 150 Volt-Microsecond. All units manufactured and tested to MIL-PRF-21038. QPL units available. Special order class V (155°C).

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These pulse transformers manufactured to MIL-STD-1553. COMMAND/ RESPONSE MULTI-PLEX DATA BUS requirements. They also are manufactured to MIL-PRF-21038/27 specifications and are designed to meet MAC AIR SPECIFICATIONS A3818, A5690, A5232, and A4905.
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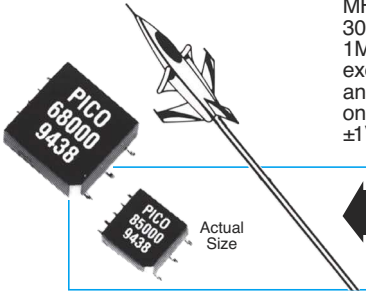

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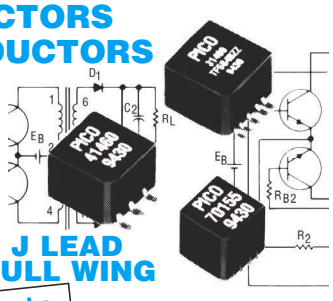

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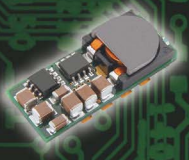

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DPA & IBA Bricks

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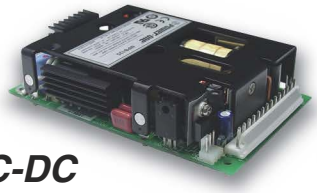
Digital Point-Of-Load Power Management and Conversion	I^2C compatible Z-7000 Series reduces power system components, traces, and development time by 90%.
	Pin-strapable Z-1000 POLs provide digital power management capabilities without software or external controllers.
Analog Point-Of-Load Conversion	Y-Series POL converters are available in industry-standard and high-performance Power-One footprints.
Board-Level DPA and IBA	The industry's broadest range of bricks, from 1/16 to full, includes bus converters, multi-output, and PoE solutions.
System-Level DPA and IBA	AC-DC front ends in hot-swap power shelf and chassis-mount configurations.
Centralized Architectures	Single and multiple output models include flexible modular solutions.
Industrial and Transportation	Rugged cassette style and DIN-Rail mount AC-DC and DC-DC products.
CompactPCI	AC-DC and DC-DC in 3U and 6U form factors.

AC-DC Front Ends



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MANUFACTURERS OFFERING UNITY-GAIN-STABLE AMPLIFIERS HOPE TO ADDRESS A WIDE MARKET AND MINIMIZE THE EFFORT OF LEARNING TO USE THE DEVICE. YET THESE VENDORS SACRIFICE A SIGNIFICANT PORTION OF THE POTENTIAL AC PERFORMANCE. LEARN WHEN TO CONSIDER DECOMPENSATED AMPLIFIERS AND WHAT THEY CAN OFFER YOU.

Designers often want to minimize amplitude error in sensor-based systems. This goal often leads to specifying the gain error of an amplifier's closed-loop gain over the frequency range of the sensor. Engineers commonly specify the bandwidth of an amplifier in terms of its −3-dB frequency, but, from a gain-accuracy point of view, almost a 30% gain error occurs at this frequency. The term "effective bandwidth" connects the frequency response of the amplifier and the gain accuracy that the application requires. You define the effective bandwidth as the bandwidth for which the gain error is less than or equal to a specified error.

EFFECTIVE BANDWIDTH

Sensors have a relatively low frequency response, and, at lower frequencies, the gain error due to finite open-loop gain is small. You can calculate the effective bandwidth to maintain an error at less than a specified value from the single-pole, closed-loop, frequency-response model of the amplifier. It would be useful to calculate the effective bandwidth from specifications such as gain bandwidth that are commonly available in a data sheet. The relationship of an amplifier's closed-loop bandwidth being equal to the gain bandwidth divided by the gain is true for noninverting amplifiers and approximately true for inverting amplifiers.

The next consideration is what basis to use in defining the maximum amplitude error. In almost all systems, the analog portion of the signal path ends at the input of an ADC, and, by extension, the resolution of the ADC defines the error of interest. This article uses an error of ½ LSB of the ADC's resolution as the maximum error. As the resolution of the ADC increases, the maximum error decreases. **Table 1** shows the ½-LSB error for ADC resolutions of 8 to 18 bits.

TABLE 1 ADC RESOLUTION VERSUS ½-LSB ERROR

ADC resolution (bits)	½-LSB error
8	1.95×10^{-3}
10	4.88×10^{-4}
12	1.22×10^{-4}
14	3.05×10^{-5}
16	7.63×10^{-6}
18	1.91×10^{-6}

To easily evaluate the effect of the single-pole model on the gain error as a function of frequency, you calculate a normalized single-pole function. This calculation places the pole at 1 Hz, which represents the −3-dB loss in closed-loop gain, with an ideal closed-loop gain of one, or 0 dB. Using this single-pole model, you calculate the frequency for a gain error less than or equal to the specified error. You can then calculate the effective bandwidth in terms of the −3-dB bandwidth of the closed-loop gain of the amplifier you are evaluating. Keep in mind that the −3-

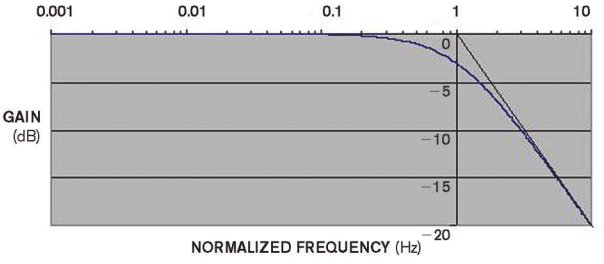

Figure 1 A single-pole function has a pole at 1 Hz.

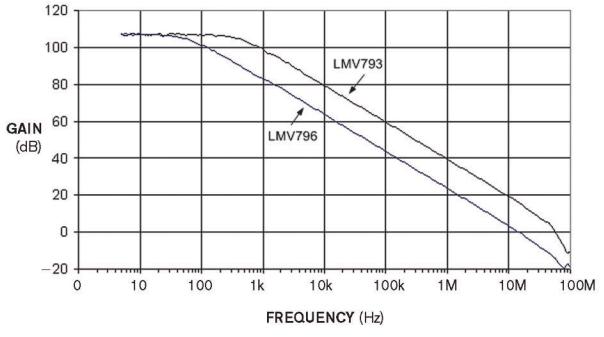

Figure 2 In this plot of the open-loop gain on a sample of the LMV796 and LMV793 amplifiers, the LMV796 displays the classic single-pole response with a pole at about 60 Hz and a unity-gain-crossover frequency of 17 MHz. The gain plot for the LMV793 shows a two-pole open-loop response due to decompensating, or undercompensating, the amplifier.

dB point is almost a 30% gain error and that the bandwidth is smaller with a lower error specification.

$$\text{GAIN}\left(\frac{V}{V}\right)=\frac{1}{\sqrt{1+\left(\frac{f}{f_C}\right)^2}}. \quad (1)$$

$$\text{GAIN (dB)}=20\log\left(\text{GAIN}\left(\frac{V}{V}\right)\right). \quad (2)$$

$$\text{GAIN ERROR}\left(\frac{V}{V}\right)=1-\text{GAIN}\left(\frac{V}{V}\right). \quad (3)$$

Table 2 shows a small section of the spreadsheet calculations to help you visualize the gain roll-off with frequency. You calculate **equations 1**, **2**, and **3** versus frequency in columns 1, 2, and 3, respectively (**Figure 1**).

The next step is to find the frequency at which the gain error is equal to a ½ LSB of an ADC with specified bits of resolution. **Equation 4** calculates the ½-LSB error, given the resolution of the ADC (**Table 1**).

$$\frac{1}{2}\,\text{LSB\_ERROR}=\frac{1}{2(2^{\text{ADC\_RESOLUTION}})}. \quad (4)$$

To calculate the frequency at which the gain error is equal to the ½-LSB error, substitute **Equation 4** into **Equation 1** and rearrange it, yielding **Equation 5**. You use **equations 4** and **5** to calculate the values in **Table 3**.

$$f(\text{AT\_}\frac{1}{2}\,\text{LSB\_ERROR})=\sqrt{\left(\frac{1}{1-\frac{1}{2}\,\text{LSB\_ERROR}}\right)^2-1}. \quad (5)$$

In **Table 3**, the column with the heading "Frequency at error" gives the frequency at which the gain error is equal to a ½ LSB of the ADC's resolution. At lower frequencies, the gain error is less than ½ LSB. This bandwidth is effective for the specified resolution. For example, the effective bandwidth of an amplifier driving a 10-bit ADC is 0.03126 of the −3-dB frequency, and the effective bandwidth of a 14-bit ADC is 0.007813 of the −3-dB frequency. If the amplifier has a closed-loop, −3-dB frequency of 100 kHz, the effective bandwidths are 31.3 and 7.81 kHz, respectively. **Equations 1** through **5**, which divide the gain bandwidth of an amplifier by its closed-loop gain, demonstrate

TABLE 2 NORMALIZED ONE-POLE FUNCTION FROM 0.1 TO 10 Hz

Frequency (Hz)	Gain (V/V)	Gain (dB)	Error at gain of one (V/V)
0.1	0.9950	−0.0432	0.0050
0.2	0.9806	−0.1703	0.0194
0.3	0.9578	−0.3743	0.0422
0.4	0.9285	−0.6446	0.0715
0.5	0.8944	−0.9691	0.1056
0.6	0.8575	−1.3354	0.1425
0.7	0.8192	−1.7319	0.1808
0.8	0.7809	−2.1484	0.2191
0.9	0.7433	−2.5768	0.2567
1	0.7071	−3.0103	0.2929
2	0.4472	−6.9897	0.5528
3	0.3162	−10.0000	0.6838
4	0.2425	−12.3045	0.7575
5	0.1961	−14.1497	0.8039
6	0.1644	−15.6820	0.8356
7	0.1414	−16.9897	0.8586
8	0.1240	−18.1291	0.8760
9	0.1104	−19.1381	0.8896
10	0.0995	−20.0432	0.9005

TABLE 3 ADC RESOLUTION AND NORMALIZED FREQUENCY AT ERROR VALUE

ADC resolution (bits)	½-LSB error	Frequency at error value
8	1.953×10^{-3}	6.259×10^{-2}
10	4.883×10^{-4}	3.126×10^{-2}
12	1.221×10^{-4}	1.563×10^{-2}
14	3.052×10^{-5}	7.813×10^{-3}
16	7.629×10^{-6}	3.906×10^{-3}
18	1.907×10^{-6}	1.953×10^{-3}
20	4.768×10^{-7}	9.766×10^{-4}
22	1.192×10^{-7}	4.883×10^{-4}

TABLE 4 EFFECTIVE BANDWIDTH FOR LMV793 AND LMV796 AT A GAIN OF 100

ADC resolution (bits)	½-LSB error	Normalized bandwidth for less-than-½-LSB error	LMV796 bandwidth at closed-loop gain of 100 (Hz)	LMV793 bandwidth at closed-loop gain of 100 (Hz)
8	1.95×10^{-3}	6.2590×10^{-2}	10,640	55,079
10	4.88×10^{-4}	3.1260×10^{-2}	5314	27,509
12	1.22×10^{-4}	1.5630×10^{-2}	2657	13,754
14	3.05×10^{-5}	7.8130×10^{-3}	1328	6875
16	7.63×10^{-6}	3.9060×10^{-3}	664	3437
18	1.91×10^{-6}	1.9530×10^{-3}	332	1719

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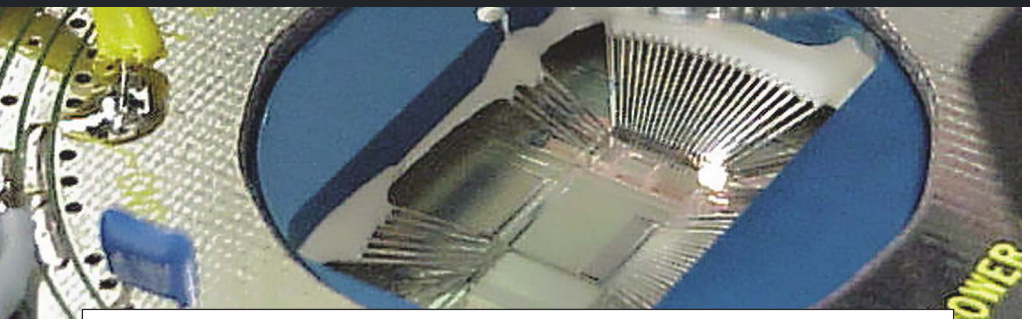

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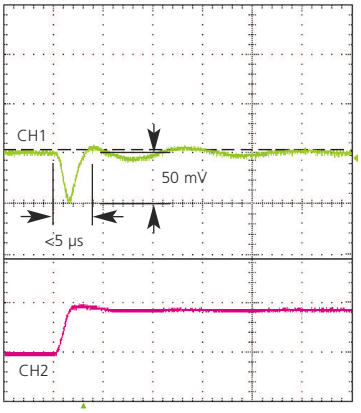
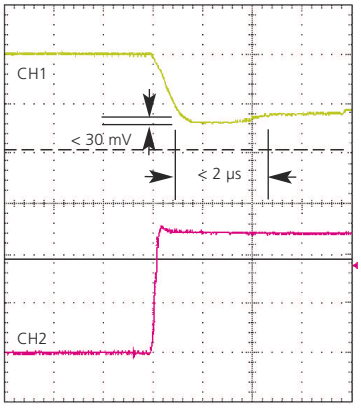


CH1: V_{OUT} 50 mV/div Timebase: 5 µs
CH2: I_{OUT} 50 A/div

48 V_{IN}, 1.2 V_{OUT}, 0-40 A at 10 A/µs
Less than 50 mV undershoot and recovery
in <5 µs using 330 µF ceramic C_{OUT}.

Load Line Recovery



CH1: V_{OUT} 100 mV/div Timebase: 1 µs
CH2: I_{OUT} 40 A/div

48 V_{IN}, 1.2 V_{OUT}, 0-100 A at 600 A/µs
Less than 30 mV undershoot and recovery
in <2 µs using 220 µF ceramic C_{OUT}.

Product Listing

PRM Model No.	V_{IN} Nominal (V)	V_{OUT} Range (V)	Output Power (W)	Efficiency @ Full Load (%)
P024F048T12AL	24	26 - 55	120	95.0
P048F048T24AL	48	36 - 75	240	96.0
P045F048T32AL	48	38 - 55	320	97.0

VTM Model No.	V_{OUT} Nominal (V)	V_{OUT} Range (V)	Output Current (A)	Efficiency @ 50% Load (%)
V048F015T100	1.5	0.81 - 1.72	100	91.0
V048F020T080	2.0	1.08 - 2.29	80	94.2
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that an amplifier's effective bandwidth is substantially less than the −3-dB frequency that the theoretical usage reports.

Considering how you are using an amplifier in the signal path can partially offset the rapid loss of effective bandwidth. Amplifiers commonly use some amount of gain to scale the signal from a sensor to the input of an ADC. In many cases, the gain is greater than 10. Using gain with an amplifier eliminates the need for unity-gain stability and reduces the amount of internal compensation the amplifier uses. The advantage of decompensating the amplifier is an increase in the available bandwidth and slew rate for the same power consumption.

COMPENSATED VERSUS DECOMPENSATED

National Semiconductor's (www.national.com) LMV793 and LMV796 use the same design except for the amount of internal compensation. The LMV796 is unity-gain-stable, and the LMV793 is decompensated for a gain of 10. **Figure 2** plots the open-loop gain on a sample of each amplifier. The LMV796 displays the classic single-pole response with a pole at approximately 60 Hz and a unity-gain-crossover frequency of 17 MHz. The gain plot for the LMV793 shows a two-pole open-loop response due to decompensating, or undercompensating, the amplifier. The plot shows the open-loop-gain shift to the right, indicating the higher frequency response of the LMV793. The first pole occurs at approximately 500 Hz, which is 440 Hz higher than that for the LMV796. A second pole occurs at 45 MHz, and the open-loop gain decreases at −40 dB per decade and crosses the 0-dB axis at approximately 56 MHz. The device achieves this increased bandwidth without an increase in power consumption.

The decompensated LMV793 has significantly more bandwidth for the same current consumption as the fully compensated LMV796. This feature can provide a power savings over using a higher frequency, fully compensated amplifier, which typically would require a higher supply current.

For the LMV793, the gain bandwidth is 88 MHz for closed-loop gains of 10 or more. A second pole occurs before the open-loop gain of 1, at approximately 51 MHz. For decompensated amplifiers, the unity-gain frequency and the gain bandwidth are no longer equal. The LMV793's minimum gain for stability without using additional external compensation is 10 or 20 dB.

The frequency-dependent closed-loop gain depends on the amplifier's gain bandwidth. Amplifier data sheets routinely specify the gain bandwidth of an amplifier, and, using the closed-loop gain of the amplifier, you can easily calculate the −3-dB bandwidth. For example, the LMV796 has a gain bandwidth of 17 MHz, and, if the closed-loop gain is 100, the bandwidth of the amplifier is 0.17 MHz, or 170 kHz, and is the −3-dB point in the amplifier's frequency response. This point also has almost 30% gain error. The decompensated LMV793 has a gain bandwidth of 88 MHz for gains greater than 10. Continuing the example at a closed-loop gain of 100, the LMV793 has a bandwidth of 0.88 MHz, or 880 kHz. The LMV793 has a gain bandwidth of 88 MHz at a gain of 10 and a slew-rate rising edge

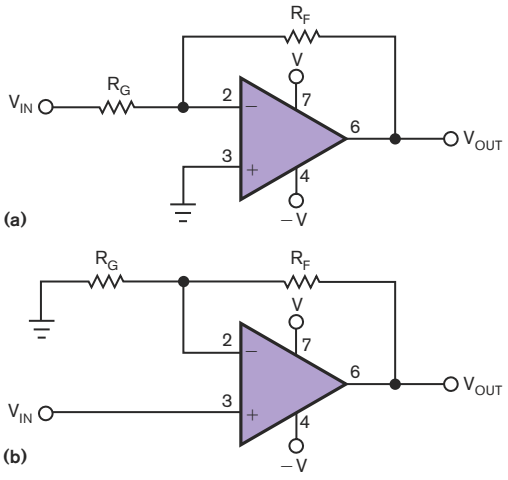

Figure 3 A decompensated amplifier offers substantially more effective bandwidth for the same power consumption and gives the designer an additional degree of freedom in amplifier selection (a). The decompensated amplifier offers additional bandwidth that can support higher ADC resolutions (b).

TABLE 5 GAIN VERSUS BETA AND BANDWIDTH

Inverting amplifier			Noninverting amplifier		
Gain	Beta	Bandwidth	Gain	Beta	Bandwidth
−1	0.500	0.500	1	1.000	1.000
−2	0.333	0.333	2	0.500	0.500
−3	0.250	0.250	3	0.333	0.333
−4	0.200	0.200	4	0.250	0.250
−5	0.167	0.167	5	0.200	0.200
−6	0.143	0.143	6	0.167	0.167
−7	0.125	0.125	7	0.143	0.143
−8	0.111	0.111	8	0.125	0.125
−9	0.100	0.100	9	0.111	0.111
−10	0.091	0.091	10	0.100	0.100

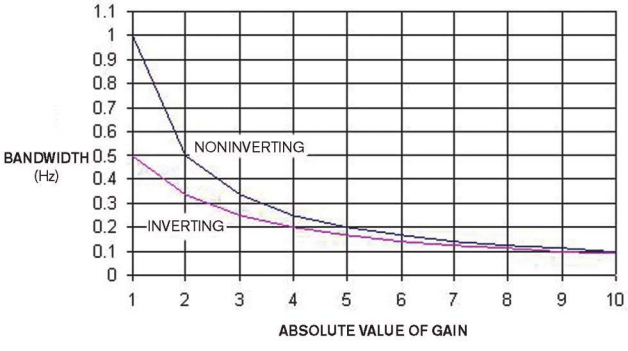

Figure 4 The bandwidth-versus-gain relationship demonstrates that, at low gains, there is significant loss of closed-loop bandwidth for the inverting amplifier.

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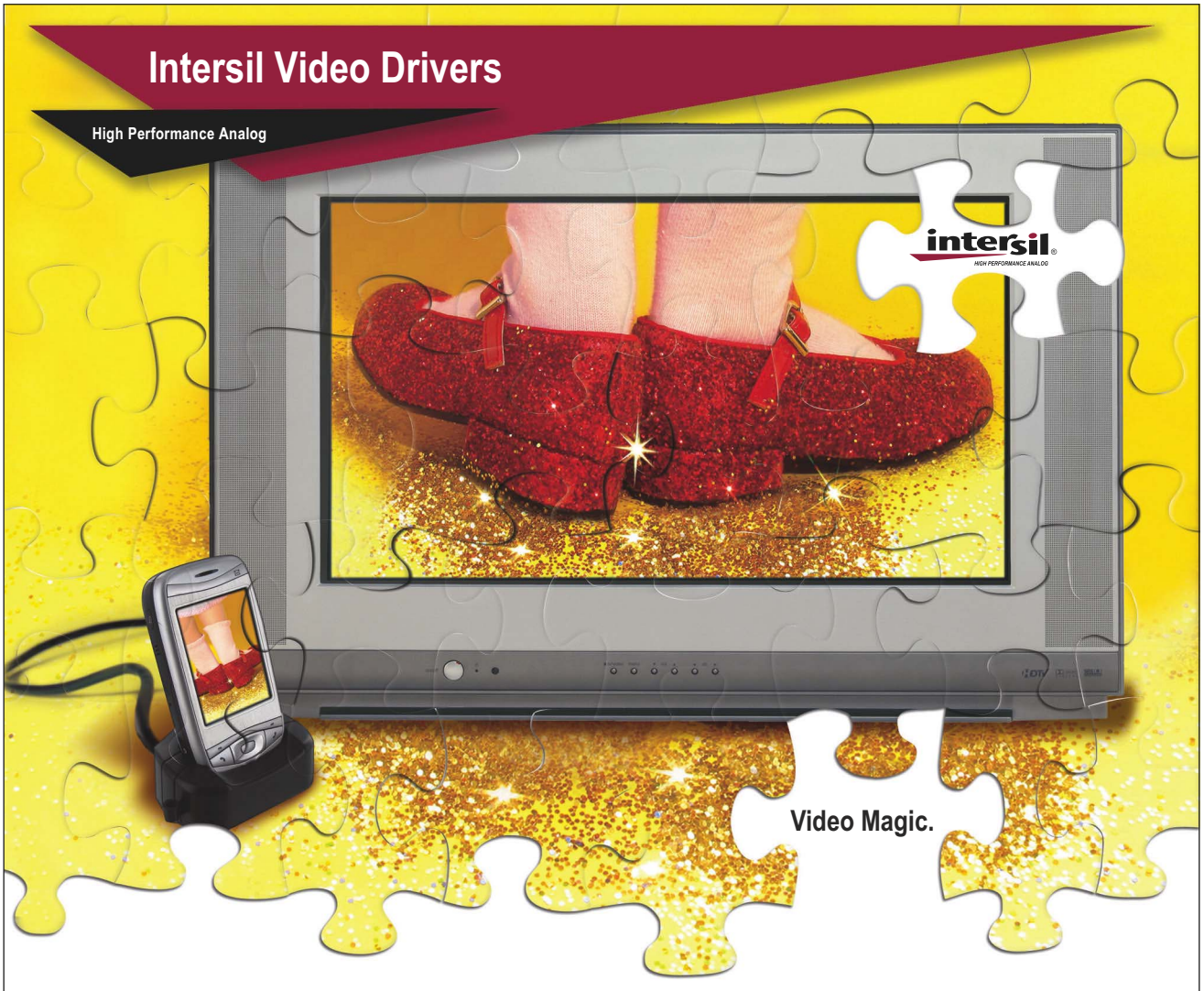

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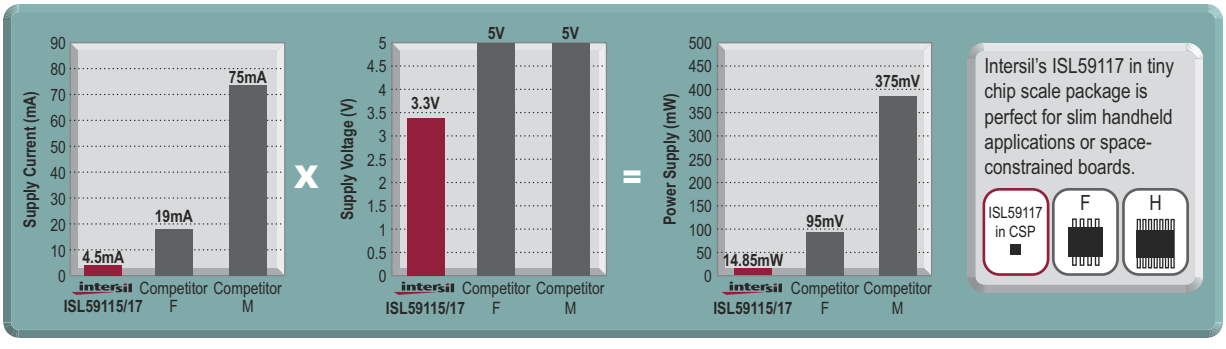

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of 40V/µsec. In contrast, the LMV796 has a gain bandwidth of 17 MHz at a gain of 10 and a slew-rate rising edge of 9.5V/µsec.

ADDED COMPONENTS AFFECT GAIN

Many sensor applications have ac-signal components that can extend to tens of kilohertz and require accurate gain over this frequency range to maintain the amplitude accuracy of the signal. To accurately amplify a signal, the design must account for gain errors as a function of frequency. **Table 4** shows the results of applying the effective-bandwidth concepts to the LMV793 and LMV796. An LMV796 with a closed-loop gain of 100 and a bandwidth of 170 kHz would have the effective bandwidth that Column 4 of the **table** shows for the range of resolutions the **table** lists. For example, at an ADC resolution of 14 bits, the effective bandwidth would be 1328 Hz. **Table 4** shows that the LMV793 with a closed-loop gain of 100 and a bandwidth of 880 kHz would have the effective bandwidth that Column 5 lists for the range of resolutions the **table** lists. This amplifier, at an ADC resolution of 14 bits, has an effective bandwidth of 6875 Hz. As this example shows, the effective bandwidth is a small fraction of the −3-dB bandwidth. A decompensated amplifier offers substantially more effective bandwidth for the same power consumption and gives the designer an additional degree of freedom in amplifier selection. The decompensated amplifier offers additional bandwidth that can support higher ADC resolutions.

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In discussions about the closed-loop bandwidth of amplifiers, engineers often apply the gain bandwidth to noninverting and inverting amplifiers to estimate the closed-loop bandwidth. **Equation 6** relates the closed-loop bandwidth to the amplifier's gain bandwidth and closed-loop gain.

$$BW = \frac{GBW}{GAIN}, \quad (6)$$

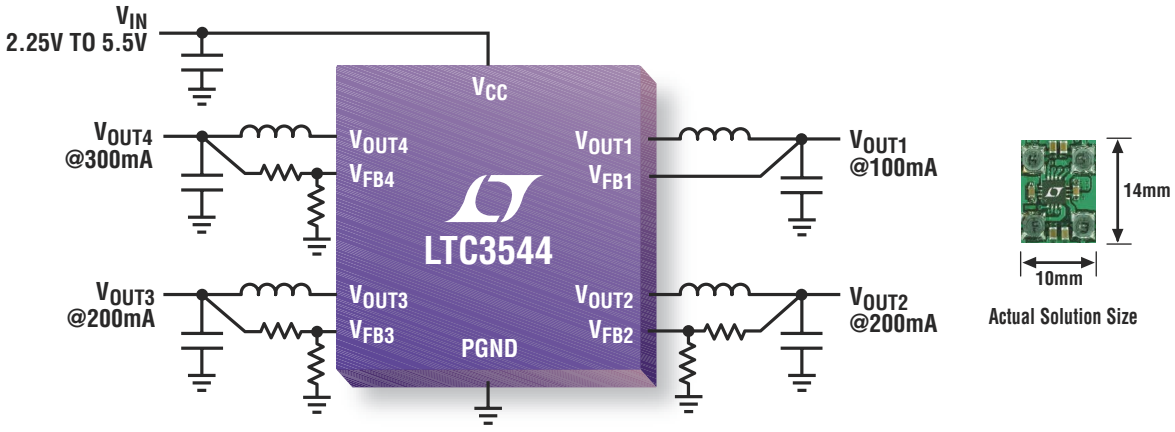
where BW is the bandwidth and GBW is the gain bandwidth.

The **equation** expresses a relationship that applies to noninverting amplifiers and approximately to inverting amplifiers. As the gain of the inverting amplifier increases, the error in bandwidth, using **Equation 6**, becomes smaller. This consideration is important when you are using different amplifier configurations. **Figure 3** shows configurations of basic inverting and noninverting amplifiers.

CONSIDER BETA

The closed-loop bandwidth of an amplifier is a function of the gain and the amount of feedback, also known as the feed-

Quad Buck



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LTC3419	Dual Synch Step-Downs	2.5V to 5.5V	0.6 x 2	0.6	2.25MHz	35	3mm x 3mm DFN-8, MSOP-10
LTC3548/-1/-2	Dual Synch Step-Downs	2.5V to 5.5V	0.8, 0.4	0.6	2.25MHz	40	3mm x 3mm DFN-10, MSOP-10E
LTC3407-2/-3	Dual Synch Step-Downs	2.5V to 5.5V	0.8 x 2	0.6	2.25MHz	40	3mm x 3mm DFN-10, MSOP-10E
LTC3417A	Dual Synch Step-Downs	2.25V to 5.5V	1.5, 1	0.8	2.25MHz	125	3mm x 5mm DFN-20, TSSOP-20E
LTC3446	Single Synch Step-Down + Dual VLDOs	2.7 to 5.5V	1.0, 0.3, 0.3	0.4	2.25MHz	140	3mm x 4mm DFN-14
LTC3545	Triple Synch Step-Downs	2.25V to 5.5V	0.6 x 3	0.6	2.25MHz	58	3mm x 3mm QFN-16, MSOP-10E
LTC3544/B	Quad Synch Step-Downs	2.25V to 5.5V	0.3, 2 x 0.2, 0.1	0.8	2.25MHz	70	3mm x 3mm QFN-16
LTC3562	I²C Quad Synch Step-Downs	2.7V to 5.5V	2 x 0.6, 2 x 0.4	0.6	2.25MHz	100	3mm x 3mm QFN-20

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back factor, beta. Beta is the portion of the amplifier's output that feeds back to the input. You calculate the beta of both configurations with the following equation:

$$\beta = \frac{R_G}{R_G + R_F}. \quad (7)$$

The beta differs for noninverting and inverting amplifiers with the same absolute value of gain due to the difference in the resistor ratios necessary to set the same absolute value of gain. **Table 5** shows the calculated beta and normalized bandwidth for gains as high as 10 and −10. **Equation 8** shows the calculation for the bandwidth of a unity-gain-stable amplifier in the inverting or the noninverting configuration:

$$BW = \frac{GBW(\beta)}{GAIN}. \quad (8)$$

Figure 4 shows the bandwidth-versus-gain relationship, demonstrating that, at low gains, there is significant loss of closed-loop bandwidth for the inverting amplifier. For example, the bandwidth of the inverting amplifier with a gain of −1 is half the bandwidth of the noninverting amplifier with a gain of 1. In these cases, if an application requires additional bandwidth at the same level of power consumption, using a decompensated amplifier is an acceptable alternative. Offsetting the additional bandwidth at lower gains is the required external compensation to prevent the amplifier from oscillating. **Figure 4** also shows the bandwidth of the inverting gain to be asymptotic to the noninverting gain as the closed-loop gain increases. To externally compensate the decompensated amplifier for low gains, refer to the LMV793 data sheet, which details various compensation techniques.

In summary, decompensated amplifiers provide an additional degree of freedom to circuit designers in meeting the performance, power, and price targets of their design. The additional circuitry that may be necessary for external compensation has little effect on overall complexity but allows a more customized design to give better overall performance. Regardless of which design you use, understanding the details and trade-offs is necessary to fully meet the required specifications. EDN

AUTHOR'S BIOGRAPHY

Walter Bacharowski is an amplifier-applications manager at National Semiconductor, where he has worked for 15 years. He has a bachelor's degree in electrical engineering from Cleveland State University and has had continuing education in engineering, management, marketing, and technology. His personal interests include electronics, model rocketry, and alternative-energy technology.

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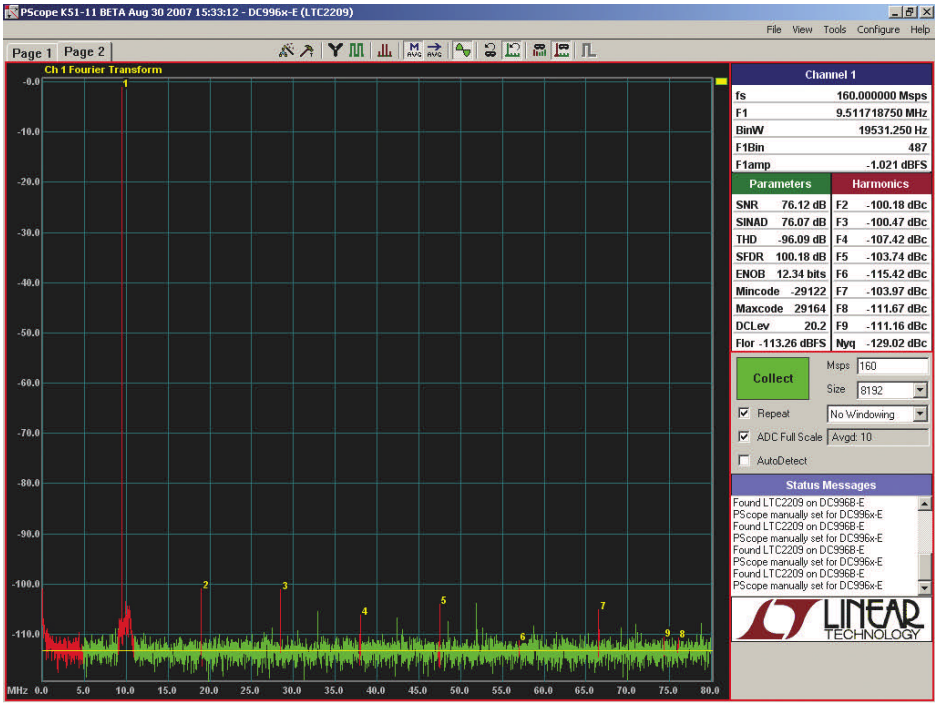

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LTC2205	65Msps	79.0dBFS	610mW
LTC2204	40Msps	79.1dBFS	480mW
LTC2203	25Msps	81.6dBFS	220mW
LTC2202	10Msps	81.6dBFS	140mW

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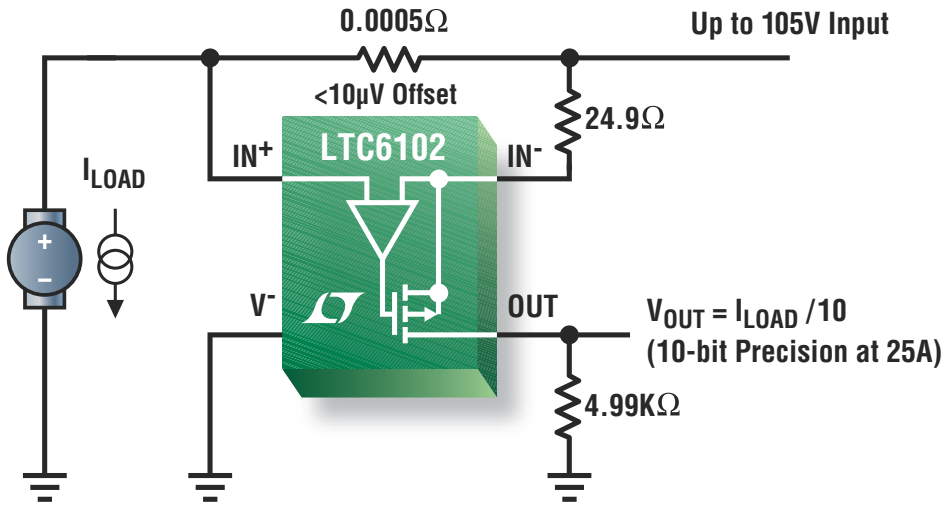

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Response Time	3.5µsec	3.5µsec	1µsec	1µsec	1µsec	1µsec	40µsec	10µsec
V_{OS} Max.	250µV	300µV	450µV	450µV	10µV	300µV	300µV	100µV
V_{OS} Drift	1µV/°C	1µV/°C	1.5µV/°C	1.5µV/°C	50nV/°C	1µV/°C	0.5V/°C	0.5V/°C
I_{BIAS} Max.	40nA	25µA	170nA	170nA	3nA	170nA	10µA	20µA
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PSRR Min.	106dB	100dB	110dB	110dB	120dB	118dB	105dB	120dB

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READERS SOLVE DESIGN PROBLEMS

Filter simplifies software-defined radio

John Wendler and Ray Tremblay, Tyco Electronics,
M/A-Com Wireless Systems, Lowell, MA

SDRs (software-defined radios) provide enormous flexibility, permitting you to change modes or waveforms at will. This Design Idea focuses on the "exciter" portion of a moderate-bandwidth SDR (**Figure 1**). The RF carrier or transmitter IF enters the quadrature modulator, and the modulated output exits for further frequency translation or amplification, depending on the details of the design. The DSP section generally works with analytic signals—in this case, signals with real and imaginary parts—at baseband. These signals may have started out as a voice speaking into a microphone that attaches to an ADC, or they may have started out as data from a computer. Regardless of the signals' origin, the DSP performs calculations on the stream of numbers, performing filtering, perhaps adding signaling tones or packetizing the data, and converting the stream into the final I and Q modulating signals. For moderate bandwidths, a stereo sigma-delta DAC or codec provides the conversion to analog signals and performs some additional filtering on the signal. Such filtering is often necessary because the quadrature modulator comprises a pair of mixers. These mixers translate any noise at baseband frequencies directly to the modulator's output.

Output noise is problematic. The FCC (Federal Communications Commission) sets spectral masks or adjacent-channel-power-ratio requirements on some services, such as land mobile radio. These requirements govern the allowed spectrum of a transmission and vary according to the bandwidth of the channel and the frequency of transmission. Their function is always the same, however: They limit the interference to other users on nearby channels to the transmitter. Meeting the spectral mask is a regulatory requirement; you cannot certify a radio without proving that it meets this requirement, and, without this certification, you cannot legally sell it. **Figure 2** shows a sample spectral mask, 47 CFR 90.210 G, with a normalized X axis to show the offset from the center of the channel and a normalized Y axis to show the unmodulated carrier output. This mask applies to the 800-MHz SMRS (specialized-mobile-radio service) in which channels are 25 kHz apart but signals can occupy only 20 kHz.

The unmodulated carrier first transmits at the center of the mask, and the top of the mask adjusts to correspond with the output power of the transmitter. You then turn on the modulation, thereby spreading the spectrum. The resulting spectrum must fall below the mask line in all places.

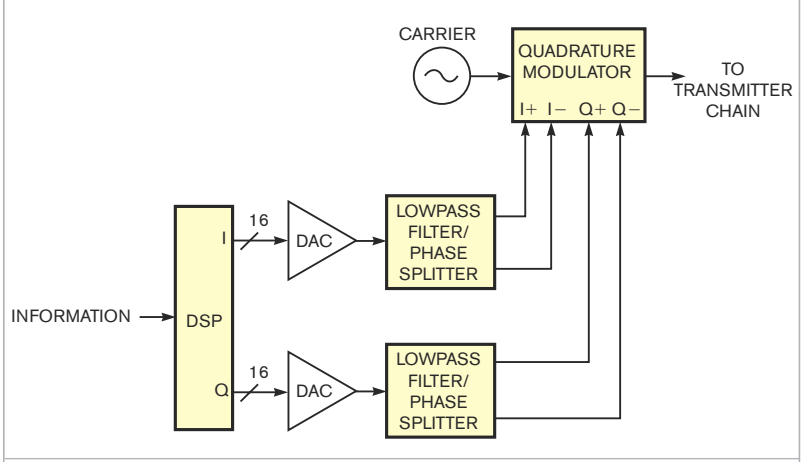

Figure 1 A pair of DACs converts the baseband signal from a DSP into I and Q signals for the quadrature modulator of a software-defined radio.

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A close examination of **Figure 2** shows some interesting features. On the carrier trace, the sampling-frequency spurs appear at ±19.2 kHz away from the center. The modulated spectrum is also interesting. The filter in the sigma-delta DAC causes the nearly vertical roll-off at approximately ±10 kHz. The mounds that appear around ±12 kHz and gradually roll off are spectral regrowth, which nonlinearities in the high-power amplifier cause.

Many moderate-bandwidth SDRs need a translator between the sigma-delta DAC's single-ended output and a typical balanced-input quadrature modulator. It is frequently desirable to follow up the DAC output with a hardware filter that removes the DAC's high-frequency noise and ensures compliance with spectral-mask requirements. Further complicating things, the optimal common- and differential-mode output voltages of the DAC are likely to differ from those that the modulator requires. An easy scaling factor does not relate common- and differential-mode voltages.

Handling all of these considerations with a conventional approach can require as many as four operational amplifiers with multiple filter sections per I or Q channel. The filters require close component matching to guarantee that carrier and single-sideband suppression—key measures of quadrature-modulator ideality—do not degrade as a function of baseband frequency. The Linear Technology (www.linear.com) LTC1992, on the other hand, addresses the problem in a single section. Linear shows a fully balanced approach to the problem in its data sheet (**Reference 1**).

It turns out, however, that a fully balanced approach is unnecessary. The circuit in **Figure 3** has excellent phase and amplitude balance between the output channels and eliminates some critical component-matching requirements. Pin 2 is set for the desired common-mode output voltage, and the DAC's midpoint voltage connects through an input resistor to Pin 8. Note that any mismatch between the input voltage and the midpoint voltage appears at the outputs and causes asym-

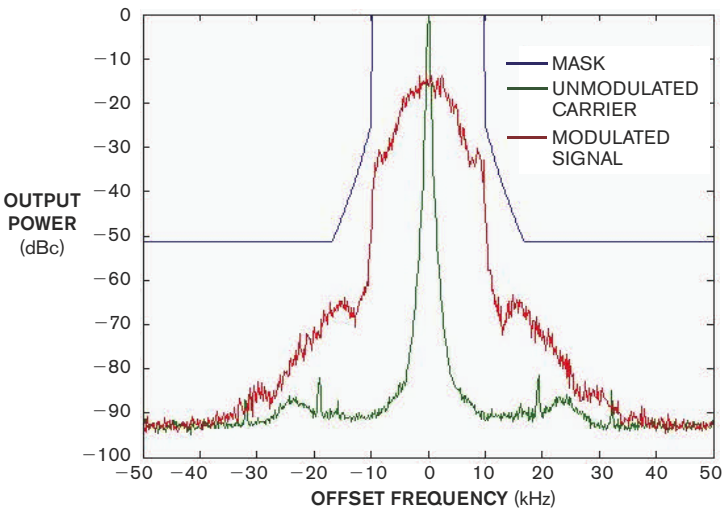

Figure 2 A sample spectral mask, 47 CFR 90.210 G, has a normalized X axis to show the offset from the center of the channel and a normalized Y axis to show the unmodulated carrier output.

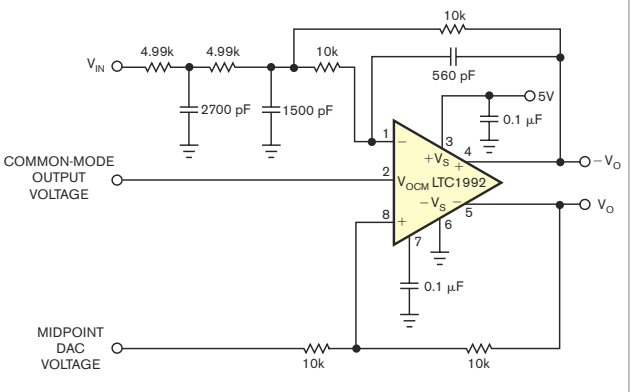

Figure 3 This circuit has excellent phase and amplitude balance between the output channels and eliminates some critical component-matching requirements.

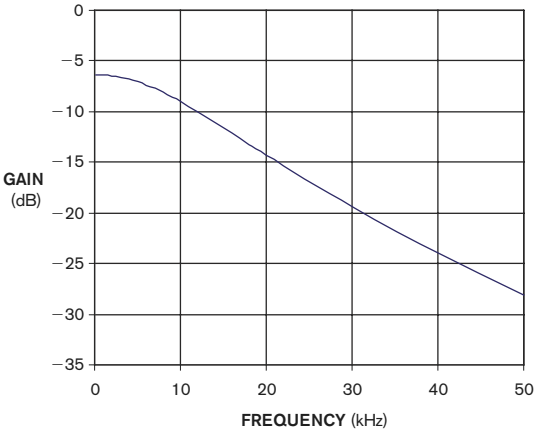

Figure 4 The measured frequency response of the positive channel with respect to ground shows an apparent 6-dB loss as a result of looking at only half the differential-output voltage; when you examine the full balanced output, the net gain is 0 dB.

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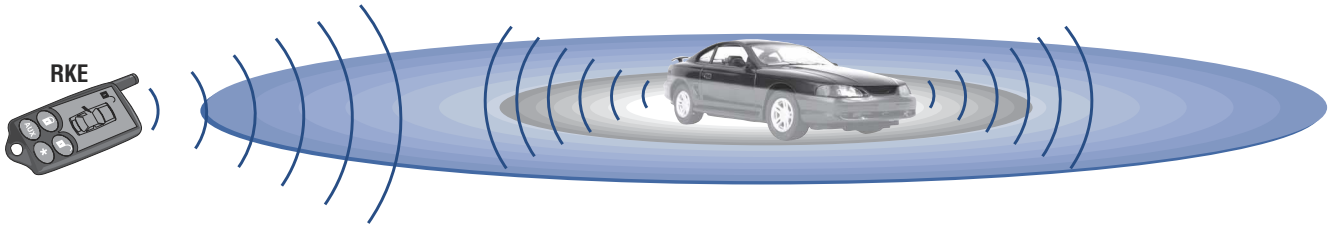

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metrical swing. This application bypasses Pin 7. The filter is a passive single-pole circuit cascaded with an inverting Sallen-Key filter, but other topologies are feasible.

Figure 4 shows the measured frequency response of the positive channel with respect to ground. The apparent 6-dB loss is a result of looking at only half the differential-output voltage; when you examine the full balanced output, the net gain is 0 dB. **Figure 5** shows the measured deviation from an ideal equal-amplitude, 180° phase shift between the positive and the negative outputs. The agreement in the critical 300-Hz to 3-kHz range is less than 0.1 dB and 0.1°. Even at 50 kHz, the error is less than 0.5 dB and 1°.EDN

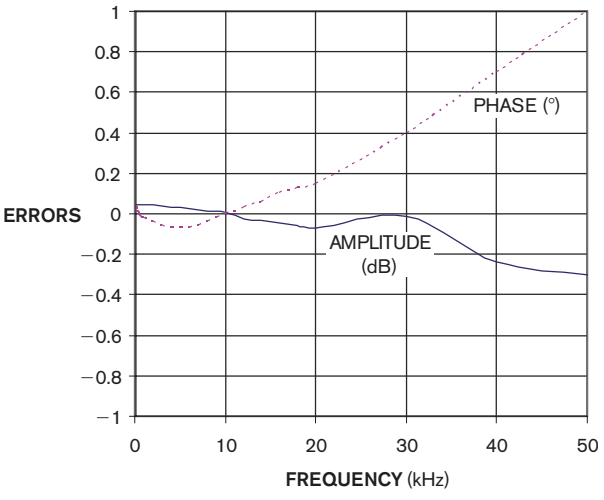

Figure 5 The measured deviation from an ideal equal-amplitude, 180° phase shift between the positive and the negative outputs shows agreement of less than 0.1 dB and 0.1° between 300 Hz and 3 kHz.

REFERENCE

1 "LTC1992: Fully Differential Input/Output Amplifier/Driver," Linear Technology, July 2003, www.linear.com/pc/downloadDocument.do?navId=H0,C1,C1154,C1009,C1126,P2348,D3455.

ACKNOWLEDGMENT

The authors gratefully acknowledge the assembly assistance of Deb Girard.

Thermoelectric-cooler unipolar drive achieves stable temperatures

W Stephen Woodward, Chapel Hill, NC

Most engineers know about the solid-state refrigerators called Peltier devices or, more commonly, TECs (thermoelectric coolers) and how they can actively cool temperature-sensitive electronic components, such as optical detectors and solid-state lasers. It's also common knowledge—although perhaps less so—that TECs are bidirectional heat pumps and can therefore both heat and cool, depending on the direction of the supplied drive current. TECs can therefore serve as the basis for precision microthermostats, maintaining a predetermined temperature against ambient-temperature excursions that range both above and below the setpoint.

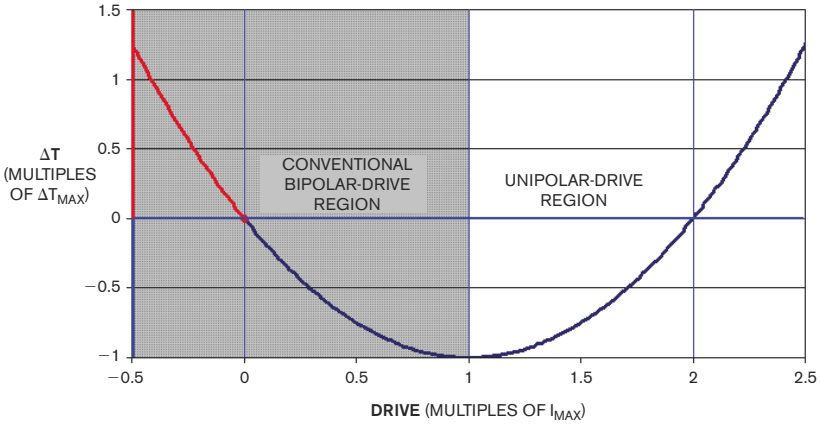

Figure 1 This plot of temperature versus maximum current shows that operating a TEC at high currents achieves heating and cooling from a unipolar drive.

The rub is that bidirectional-TEC drive tends to be an inconvenient design problem. It requires either dual bipolar power supplies or relatively complex H-bridge-drive output circuits involving arrays of power transistors that selectively reverse the TEC excitation as the required direction of heat flow dictates. But an alternative method offers advantages whenever simplicity matters more than efficiency. This Design Idea presents a novel approach to bidirectional-TEC-temperature control that avoids both the inconvenience of dual power supplies and the complexity of bidirectional drive. It works by exploiting a little-known quirk of all TECs: the inherent reversal of net heat flow at unconventionally high levels of drive current.

LINEAR TECHNOLOGY

DESIGN NOTES

8A Low Voltage, Low Profile DC/DC µModule Regulator in 9mm × 15mm Package Weighs Only 1g

Design Note 430

Eddie Beville and Alan Chern

Introduction

In communications, industrial and other high power systems, board-mounted point-of-load (POL) DC/DC power supplies simplify thermal management and offer high performance. An ideal POL power supply module takes a minimal amount of space and mounts on the board much like other surface mount ICs without special tooling. It should also demonstrate exceptional thermal performance with excellent efficiency and low power dissipation.

8A DC/DC µModule™ Regulator in an IC Form Factor

The LTM4608® µModule regulator is a complete high density power supply in a low profile (15mm × 9mm × 2.8mm) LGA surface mount package (Figure 1). Its small form factor houses the switching controller, MOSFETs, inductor and all support components, and weighs only 1g. At this size, it can be mounted on the back side of a system board, taking advantage of otherwise unused space.

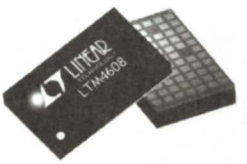

Figure 1. The LTM4608 Offers High Power Density in a 9mm × 15mm × 2.8mm LGA Package

The LTM4608 operates from an input supply range of 2.375 to 5.5V, and a single resistor is all that is needed to set the output voltage within a 0.6V to 5V output range. Its high efficiency design and low thermal impedance package delivers up to 8A continuous current.

Wealth of Features

The LTM4608's 1.5MHz switching frequency and current mode architecture allow it to react quickly to line and load transients without sacrificing stability. Cycle-by-cycle current mode control also enables excellent current sharing for parallel operation. The integrated clock enables multiphase operation and frequency synchronization, and a frequency spread spectrum feature can also be activated to further reduce switching noise harmonics. The device supports output voltage tracking or simpler supply rail sequencing. Programmable output voltage margining is supported for ±5%, ±10%, and ±15% levels. Fault protection features include over voltage protection, over current protection, and thermal shutdown.

Quick and Easy Design

Figure 2 shows a typical 1.8V output design; its efficiency is shown in Figure 3. Because the LTM4608 includes two integrated 10µF ceramic capacitors, additional input capacitors are only needed for large load steps up to the full 8A level. Linear Technology provides a µModule

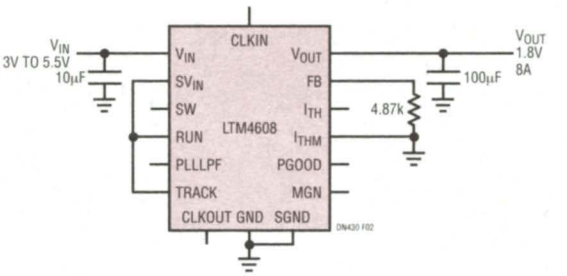

Figure 2. Few Components Are Required for a 1.8V/8A Application

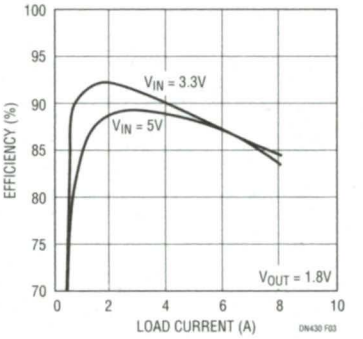

Figure 3. Efficiency of the Application in Figure 2

Power Design tool and SwitcherCAD™ simulation tool to calculate the necessary capacitance for any particular design (www.linear.com/micromodule).

For low output voltage ripple and low droop during load transients, low ESR capacitors should be used. A low ESR polymer or ceramic capacitor is sufficient. Typical ranges are 100µF to 200µF. The output voltage is set with an external resistor from the FB pin to ground.

Thermally Enhanced Packaging

The LTM4608's package has a low thermal resistance of 7°C/W junction-to-pin and 25°C/W junction-to-ambient when mounted on a four-layer board with no airflow. The device's unique packaging allows simple heat sinking from both the top and bottom, making it possible to use a metal chassis as a heat sink.

Output Voltage Tracking

Output voltage tracking is programmed via the Track pin. The slave output can be tracked up and down with another regulator's output.

Current Sharing: 8A + 8A = 16A

Two or more LTM4608 µModule regulators can be paralleled to provide multiples of 8A of load current. Because of the LTM4608's current mode architecture, the output current and power are evenly and safely distributed across each LTM4608. Figure 4 shows a 16A design that also operates 180° out-of-phase to reduce input and output ripple current.

Fault Conditions: Overcurrent Limit and Thermal Shutdown

The LTM4608's current mode control inherently limits cycle-by-cycle inductor current, not only in steady state operation, but also in transient. The LTM4608 device has over temperature shutdown protection that inhibits switching operation above 150°C.

Conclusion

Weighing 1g, occupying 135mm^2, and standing only 2.8mm tall, the LTM4608 is a complete and efficient point-of-load DC/DC system that eases circuit and layout challenges by fitting in the tightest spaces even on the bottom of the PCB. With the LTM4608, the design of an 8A switchmode regulator is as simple as a linear regulator. This DC/DC µModule regulator is rich in features and provides circuit protection as well as capability to current share for applications requiring more than 8A.

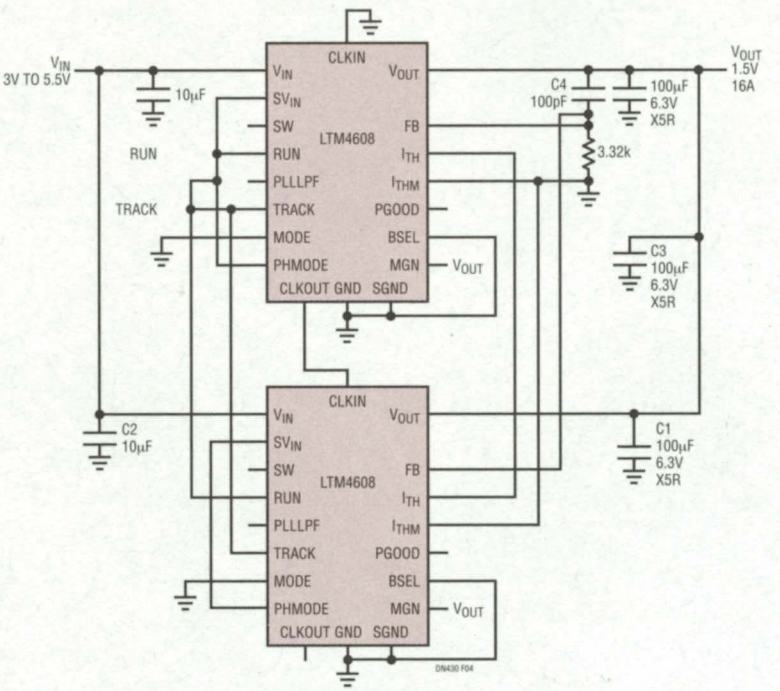

Figure 4. Two LTM4608s in Parallel, 1.5V at 16A

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The specifications of every TEC include I_{MAX}, the drive current that results in maximum net cooling. Plotting heat transfer versus drive current relative to I_{MAX} results in a typical parabolic curve (**Figure 1**). The left-hand, gray half of the plot in the **figure** shows the usual bipolar TEC's operating region, which confines drive current to the range of $-0.5\times I_{MAX}<I<I_{MAX}$. The right-hand half shows the region of interest, in which the same bipolar-temperature excursion results from unipolar-current drive: $I_{MAX}<I<2.5\times I_{MAX}$. Operation of the TEC in this second operating region thus allows bidirectional temperature control without the complexity of bidirectional-current drive.

Figure 2 shows an implementation of the concept in a high-performance PID (proportional-integral-derivative)-feedback loop. The component count is less than one-fourth that of a comparable bipolar-drive design. Feedback stability is robust, and settling time is short. The downside is a current draw as much as 150% higher than that for a conventional bipolar driver, which limits the technique to applications in which power consumption and heat dissipation aren't critical priorities and small TECs are adequate. EDN

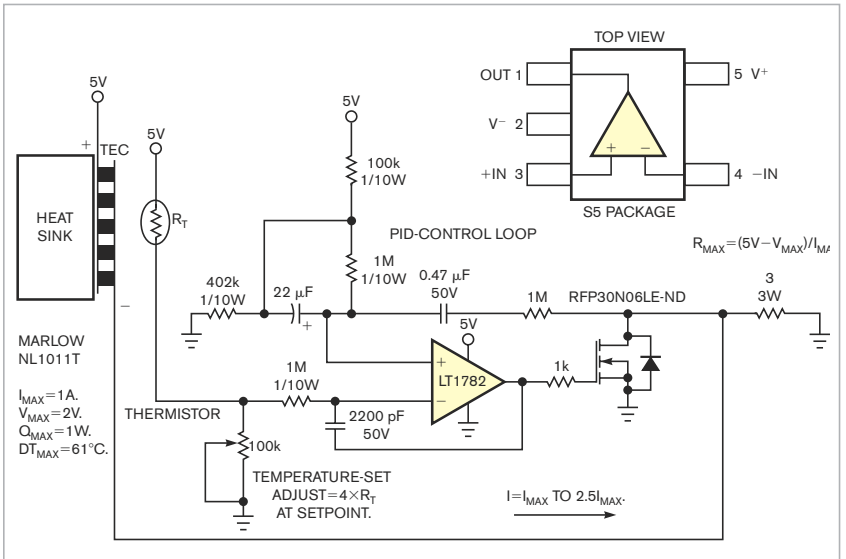

Figure 2 This circuit puts unipolar drive in a PID-feedback loop to stabilize the temperature of the target device.

Transimpedance synchronous amplification nulls out background illumination

Stefano Salvatori and Gennaro Conte, University Roma Tre, Rome, Italy

Light sensors find use in a host of important applications, spanning from consumer electronics, such as ambient-light measurements and exposure control for cameras, to scientific instruments, such as optical-absorption spectroscopy, IR (infrared) detection for thermography, and two-color pyrometry. For example, in optical spectroscopy, a correct intensity measurement of the probe beam is fundamental during material and device characterization. You must eliminate any influence that dc or very-low-frequency background light induces. Also, to increase the SNR (signal-to-noise ratio), you can apply narrowband, phase-sensitive, or lock-in detection techniques to mechanically chopped or otherwise modulated probe-light sources.

In this Design Idea, the reference signal from the light chopper as a square wave of frequency, f_{CHOP}, modulates the gain of an op-amp-based inverting amplifier (**Figure 1**). The amplifier input is a voltage proportional to the photocurrent signal produced by a photodiode, which is irradiated by a modulated light beam at the same chopper frequency. In this case, because the gain and input are at the same frequency content, a dc component, which a low-pass filter can easily detect, is present at the amplifier's output.

Op amps A_{1A} and A_{1B} convert the photogenerated current into a voltage including only the ac components. You can change the value of R_1 depending on the light level you want to detect. Neglecting A_{1A}'s input capacitance, the value of C_1 strongly depends on the terminal capacitance of the input photodiode, and you must select the value to ensure the stability of the transimpedance circuit (**Reference 1**).

The heart of the system, op amp A_{1C}, includes photoresistor R_{PR}, which represents the feedback element that determines the gain of the stage. The value of R_{PR} depends on the light that D_1 emits. A_{2B}, a voltage-to-current converter, drives D_1. The converter has a fixed voltage, V_B, and a ΔV signal through A_{2A} and A_3. A_{2A} determines the dc value of R_{PR}, whereas A_{2B} and ΔR_{PR} change at the same frequency as the reference signal. The A_3 Schmitt trigger converts any TTL/CMOS level of the reference signal into a balanced ±4.6V square wave attenuated to ±0.5V to generate an LED current change of approximately 1.8 mA p-p. For the photoresistor, R_{PR}, and LED elements, a Silonex (www1.silonex.com) CdS (cadmium-sulfide) NSL-19M51

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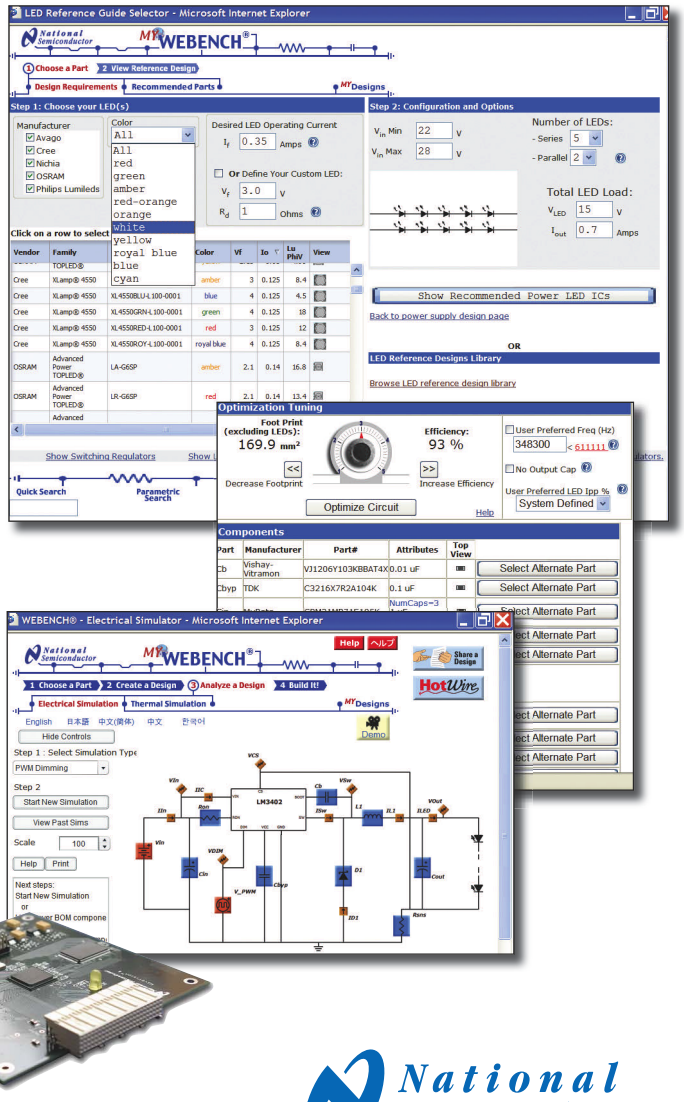

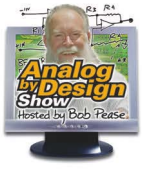

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cell couples to a red LED and resides in a black box to ensure the absence of background light on the optocoupler.

To calibrate the circuit, first disconnect or obscure the input photodiode so that A_{1A} converts no ac signal. Then, switch S_1 to the "measure" position and adjust R_{T2} to null any voltage offset referred to the output voltage. When the A_{1B} buffer generates the known approximately 300-mV test voltage and S_1 is in the calibrate position, adjust R_{T1} to fix the output voltage at 0V. In such a case, V_B voltage can set the $R_{PR}/R_C=R_A/R_B$ condition. EDN

REFERENCE

1 Wang, Tony, and Barry Erhman, "Compensate Transimpedance Amplifiers Intuitively," Application Report SBOA055A, Texas Instruments, 1993, focus.ti.com/lit/an/sboa055a/sboa055a.pdf.

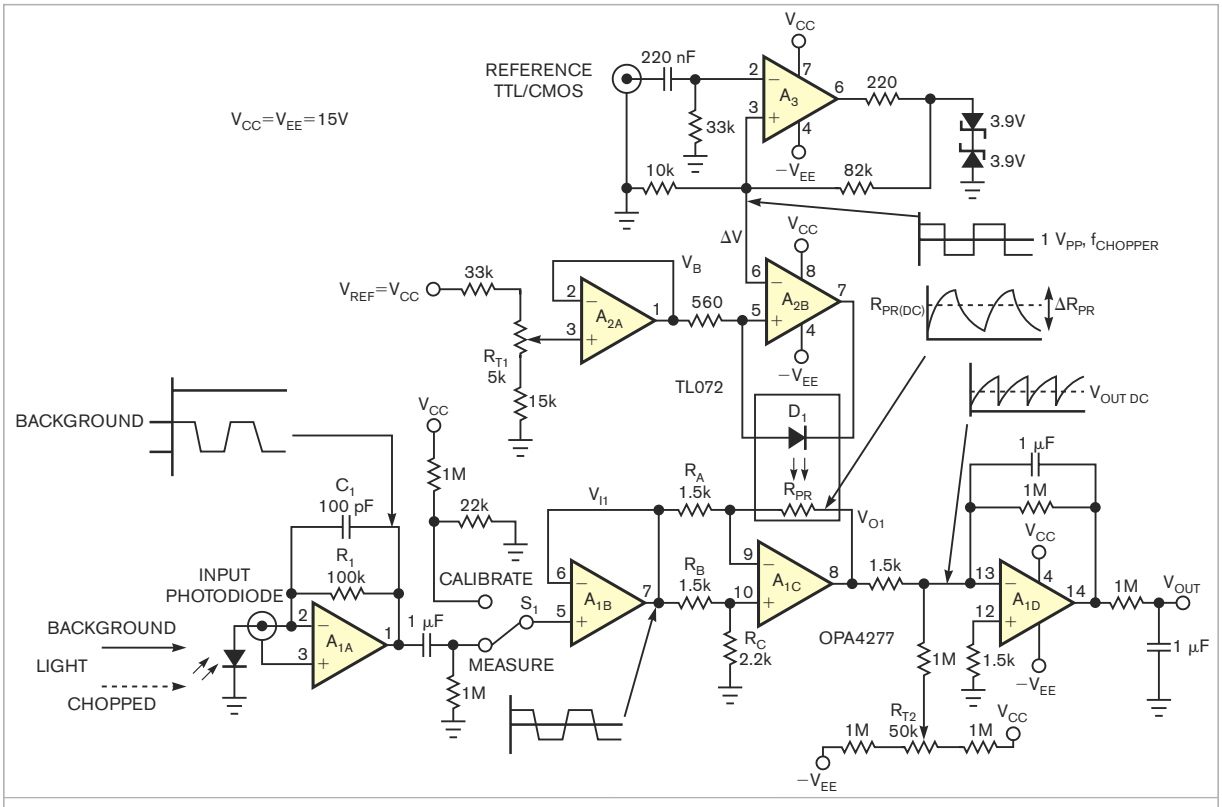

Figure 1 The reference signal from a light chopper acts as a square wave of frequency and modulates the gain of an omp-amp-based inverting amplifier.

Microcontroller drives LCD with just one wire

Noureddine Benabadji,
University of Sciences and Technology, Oran, Algeria

HD44780 LCDs are the most popular alphanumeric displays in embedded systems. The only downside is that they use six I/O pins in 4-bit nibble mode and as many as 11 pins in 8-bit mode. Earlier Design Ideas have described many approaches to saving or expanding I/O pins (**references 1**, **2**, and **3**). In driving an HD44780-compatible LCD, it would be better to use a baseline microcontroller instead of logic chips, because the microcontroller is lower cost, uses less board space, and has programming features. Microchip (www.microchip.com) has introduced the smallest PIC10F microcontroller family, which comes in a six-pin SOT-23 package.

The circuit in **Figure 1** proves useful for any pin-limited embedded system that must interface with an HD44780-compatible display through a one-wire serial link using an asynchronous, simplified RS-232 protocol at 9600 baud. It uses a PIC10F202, but any member of the PIC10F family is suitable, because the highly optimized source code in **Listing 1**, which is available with the Web version of this Design Idea at www.edn.com/071203di1, allows the program code to take fewer than 256 words. It is useless to try higher baud rates than 9600, because the PIC10F202 uses an RC internal oscillator with 1%-frequency tolerance, and the LCD requires a delay as long

as 1.6 msec for some instructions, such as "clear display."

Listing 1 is the fully commented assembler source code for the LCD232 module; the main routine consists of the display of a 2-sec-delay "splash screen," and then it enters an endless loop to wait for 1 byte as a command for the LCD, a maximum of 16 bytes as data for the LCD, and an ASCII zero. For test purposes with an external PIC microcontroller embedded system, **Listing 2**, also available at www.edn.com/071203di1, is a simple assembler source code, which sends another splash screen. EDN

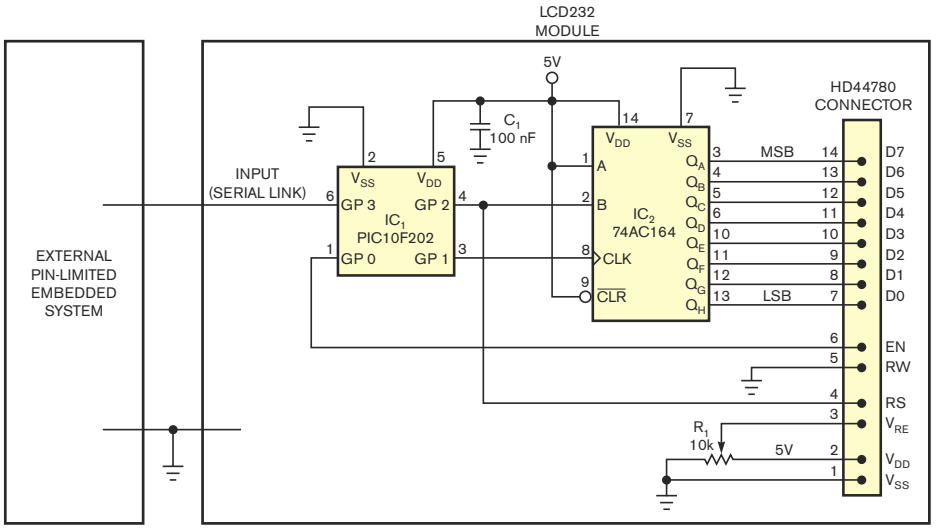

Figure 1 This circuit interfaces a pin-limited embedded system with an HD44780-compatible display through a one-wire serial link using an asynchronous, simplified RS-232 protocol.

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1 Raynus, Abel, "Squeeze extra outputs from a pin-limited microcontroller," *EDN*, Aug 4, 2005, pg 96, www.edn.com/article/CA629311.

2 "Microcontroller provides low-cost analog-to-digital conversion, drives seven-segment displays," *EDN*, May 10, 2007, pg 80, www.edn.com/article/CA6437954.

3 Niven, Rex, "RC lowpass filter expands microcomputer's output port," *EDN*, June 21, 2007, pg 74, www.edn.com/article/CA6451248.

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supplychain

LINKING DESIGN AND RESOURCES

Demand still high for 8-, 16-bit microcontrollers

As the industry continues its move to 32-bit microcontrollers, demand from the electronics supply chain is still not only solid for 8- and 16-bit varieties, but growing, according to industry sources.

Microchip Technology (www.microchip.com), which on November 5 released its first family of 32-bit devices and based it on MIPS32 architecture, for one, will not abandon the 8- or 16-bit markets any time soon. "We continue to see strong growth in the 8-bit market," says Patrick Johnson, director of Microchip's high-performance-microcontroller division. "In 16-bit [devices], we just started to bring out those [microcontroller] products that went into production in 2004."

Although Microchip's 32-bit PIC microcontroller line adds more functions and will have an approximately 15% price increase compared with the company's 16-bit PIC line, Johnson says the 16-bit microcontrollers still garner customer attention.

Microchip introduced the 32-bit PIC microcontroller line in November.

He also notes the low-price advantages 8-bit microcontrollers offer and the new opportunities that have arisen from those advantages, including low-end medical electronics. But at some point, says Jack Browne, vice president of marketing at MIPS Technologies (www.mips.com), the price difference between the three bit groups could be so insignificant that the savings won't outweigh the additional functions 32-bit microcontrollers bring to the table.

The best approach to current market demand and near-term demand, says Browne, is even microcontroller supply-chain coverage.

"Inside the 32-bit market, we look at automotive as the highest performance market, we look at the industrial market as kind of the midperformance, and the multipurpose markets are the lowest price markets. They'll ship two times the units of the automotive market, but they'll only generate half the revenue. We want to play in that whole space," he says.

GREEN UPDATE

DESIGN CHALLENGES GO GREEN

Freecale Semiconductor (www.freescale.com) is the latest company to announce a design challenge targeting green electronics. The Austin, TX-based company has invited embedded-systems engineers and engineering students to participate in its first FTF (Freescale Technology Forum) Design Challenge for green-electronics designs that use a select group of technologies from the company's portfolio. The Americas FTF Design Challenge is open to engineers and students in the United States, Canada, and Mexico. All entrants for the contest must submit their designs by Jan 31, 2008. Freescale is offering a top prize of $10,000. The company is hosting Design Challenges in Israel, Japan, Europe, India, and China over the next six months. Regional first-place winners will compete against each other in Freescale's Grand FTF Design Challenge for $50,000 and a ticket to any 2009 FTF. For more information, see www.freescale.com/designchallenge.

Premier Farnell (www.premierfarnell.com) and its US arm Newark (www.newark.com) announced a similar green-design contest in May called Live Edge (Electronic Design for the Global Environment, www.live-edge.com). More than 3200 design engineers, students, and academics from 102 countries have registered to submit designs for a product that uses electronic components and positively impacts the environment. The companies will present the 2007 Live Edge awards online Jan 31, 2008. The winner will receive $50,000, as well as a support package of $50,000 to move the design toward production.

OUTLOOK

COMPONENT SHORTAGES TO HURT HANDSET-UNIT GROWTH

The traditionally high sales quarter for the handset market may face some obstacles this fourth quarter. Strategy Analytics (www.strategyanalytics.net) has reported that it expects component shortages to have a minor impact on the global handset market. The company sees shortages in LCDs and possibly in memory and front-end components.

According to company research, global mobile-phone shipments grew 12% year over year to reach 285 million units in the third quarter. Strategy Analytics notes that Samsung (www.samsung.com) is the fastest growing top-five brand, with 47% annual-shipment growth, and Nokia (www.nokia.com) has the highest operating margin among all vendors, with a 22% rate in its handset division. Samsung's and Nokia's exceptional growth comes at the expense of other vendors, the company reports.

"Samsung is rapidly picking up share in 3G feature phones, where Sony Ericsson [www.sonyericsson.com] has seen much recent success, while Nokia continues to outsell Motorola [www.motorola.com] in the entry-tier GSM [global-system-for-mobile-communications] segment of emerging markets," says Bonny Joy, a Strategy Analytics analyst.

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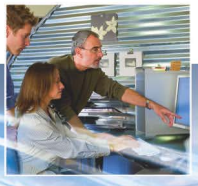

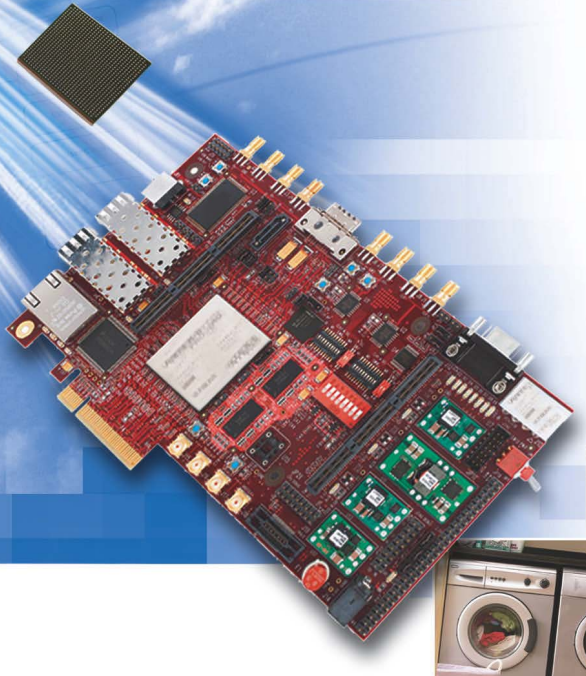

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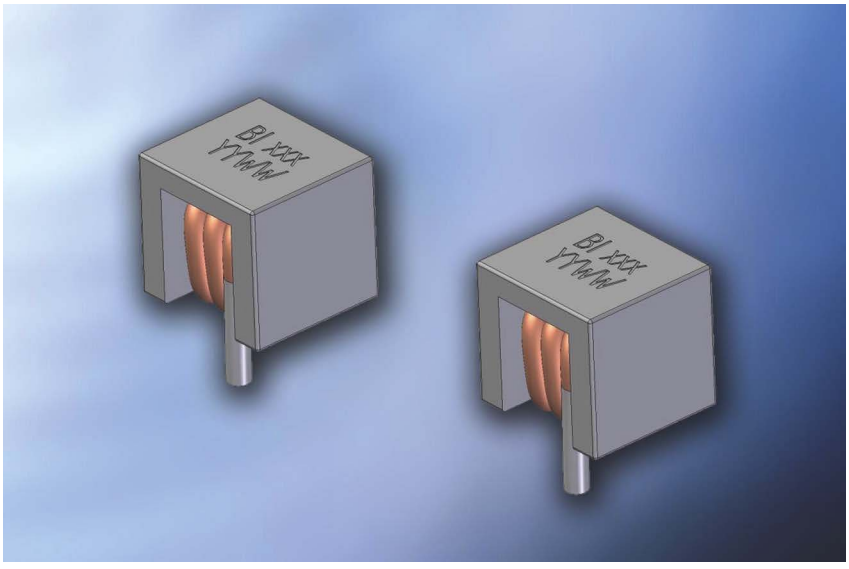

High-frequency inductor targets automatic-pick-and-place applications

The HM58 series high-frequency inductor suits 1-MHz high-frequency applications. The inductor features a thick coil wire rated for 60A saturation current and three open sides allowing a designated device aiming at automatic pick-and-place equipment. Additional features of the high-current-cube inductor include 0.22- to 2-µH inductance values, a ±3% DCR (dc-resistance) tolerance, and a −40 to +125°C operating temperature. The HM58 series costs 59 cents (10,000).

BI Technologies, www.bitechnologies.com

Z-Foil voltage divider has 25,000V ESD rating

The DSMZ ultrahigh precision Z-Foil surface-mount voltage divider features a ±0.05 ppm/°C TCR (temperature coefficient of resistance) of 0 to 60°C and a ±0.2 ppm/°C TCR of −55 to +125°C. A voltage divider provides a matched pair of Bulk Metal Z-Foil resistors. Additional features include a load-life stability of ±0.005% for 2000 hours at 70°C; a 100Ω to 10,000-kΩ resistance per resistor; a 0.05W power rating at 70°C; and the ability to withstand 25,000V ESD (electrostatic discharge). The device provides a 1- to 10-nsec rise time, depending on resistance values, without ringing and a noninductive, non-hot-spot-design. Available in a 4.06×2.69×1.6-mm, surface-mount package, the DSMZ costs $7.

Vishay Intertechnology, www.vishay.com

Supercapacitors deliver 100 times the power of batteries

The high-temperature HS and HW series of supercapacitors provides a 4.5 to 5.5V operating voltage and a higher boiling-point electrolyte, extending the operating- and storage-temperature ranges from 75 to 85°C. The vendor claims that the devices deliver 100 times the power of batteries and store 10,000 times more energy than conventional capacitors. Featuring a 28.5×17-mm footprint, the

HW series combines a 0.4F capacitance with a 100-mΩ ESR (equivalent-series resistance) at 5.5V. The HS series features a 39×17-mm footprint, and combines a 0.7F capacitance at with 55-mΩ ESR at 5.5V. The devices have a 20A pulse current with a 4A-rms, 71.7-kW/L power densities, and 5.5-kJ/L energy densities. Available in a 0.9×2.9-mm package, the HS and HW series supercapacitors cost $2.

Cap-xx Ltd, www.cap-xx.com

Thin-film-wire-chip resistors have a gold-plated-over-nickel barrier

The RNCW series of thin-film wire-bondable chip resistors feature a gold-plated-over-nickel-barrier wire-bondable surface termination. Using thin-film technology, the device provides 0.1% tolerances and a 25-ppm TCR (temperature coefficient of resistance). Available in 0402 and 0201 sizes, the RNCW sells for 20 to 50 cents in 7-in. reels (10,000).

Stackpole Electronics, www.seielect.com

Crystal oscillators provide options for multiple designs

Targeting battery-powered applications, the MOFLP series of low-power OCXO (oven-controlled crystal oscillators) features AT-, SC-, or IT-cut-crystal-design options. The devices have a 120-mA typical current consumption during start-up and 70-mA in steady-state operation at 25°C for a 3.3V-dc unit. Customers can specify a 5V operating voltage, 1- to 125-MHz frequency range, and −40 to +85°C temperature range. Available in a DIP-14; a gull-wing, surface-mount version; or an SMD configuration, the OCXO costs $100 (100) for units with frequencies lower than 40 MHz.

MMD Components, www.mmdcomp.com

Chip resistors provide low resistance and high power

Suiting high-current-sensing applications, the 3W, surface-mount LRF3W chip-resistor series targets fuel-gauging and overcurrent detection, ac/dc power supplies and VRMs (voltage-regulator modules), motorized seats, power windows, seat heaters, and automatic-fuel-pump-collision cutoff. Features include a ±100 ppm/°C TCR (temperature coefficient of resistance); a −55 to +150°C temperature range; and a 0.002 to 0.1Ω resistance range with ±1, ±2, ±5, ±10, absolute tolerances. Available in a 1225 package, the LRF3W series costs 20 cents (1800).

IRC, www.irctt.com

MICROPROCESSORS

Embedded-processing platform includes a 32-bit processor

Using the enhanced 32-128-bit Core Connect PLB (processor-local bus), the MicroBlaze 32-bit embedded-processing platform provides a configurable MMU (memory-management unit) supported by the Embedded Design Kit Version 9.2. LynuxWorks' BlueCat Linux Version 2.6 provides support for the MicroBlaze processor and the PowerPC405 processor embedded in Virtex-4 FX devices. New instructions boost the performance of the configurable processor's coupled FPU (floating-point unit), which converts between floating-point and integer operation. Enhancements to the PLB architecture allow scaling from 32-, 64-, and 128-bit interfaces. The PLB is also configurable for shared and point-

RENESAS R8C Tiny

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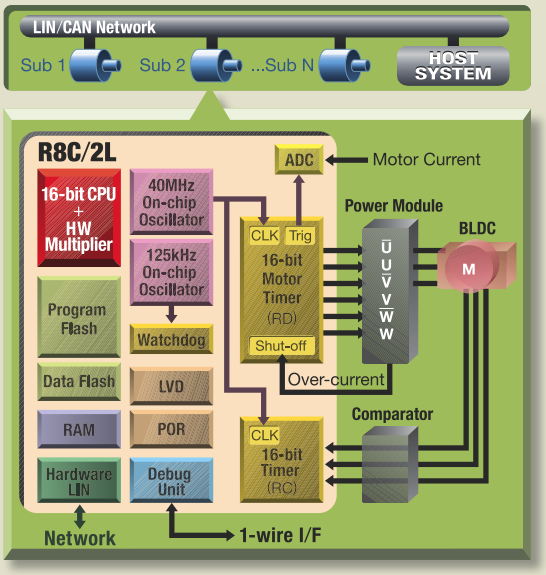
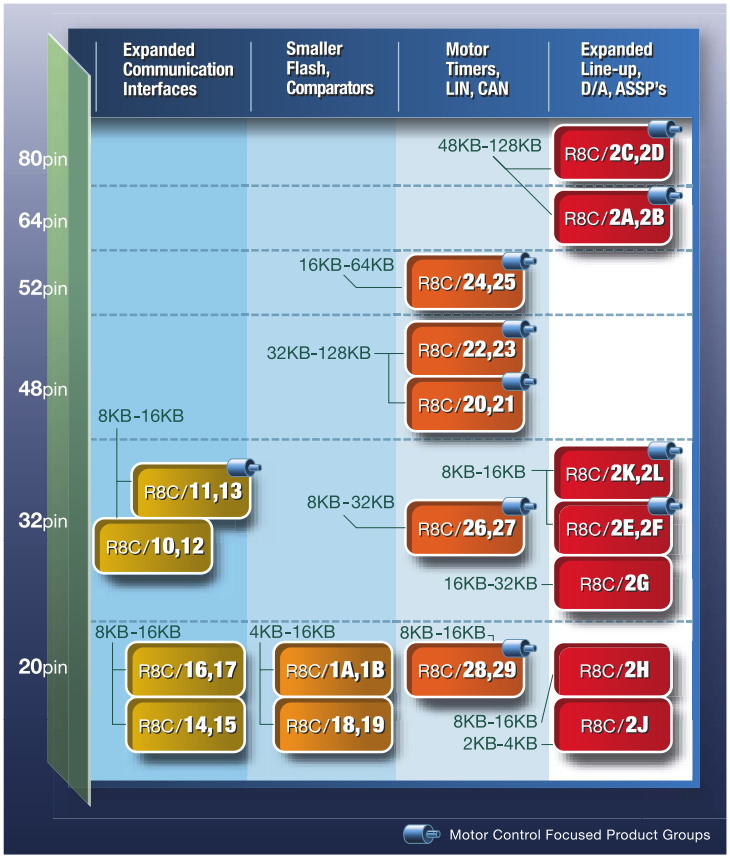


Top Reasons For Selecting R8C/Tiny's Motor Control Solutions

- **High-Performance**
  - 16-bit CPU core with hardware multiplier
  - Up to three 16-bit timers with 40MHz clock
  - 3.3µs ADC conversion with timer-trigger start option
- **Advanced Motor-Tuned Timers**
  - Up to 6-ch complementary PWM signals with independent compare registers
  - Programmable Dead-Time Control (16-bit)
  - Selectable buffer operation for fast timer reload
  - PWM signal shut-off using external trigger
- **High Component Integration**
  - Integrated LIN and CAN modules for networking
  - Watchdog with dedicated On-chip Oscillator
  - Power-on Reset, Voltage Detection Circuits and Data Flash
- **Outstanding Development Support**
  - Multiple motor control algorithms
  - Demonstration and reference design platforms

R8C/Tiny Product Lineup



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productroundup

MICROPROCESSORS

to-point connections to the high-performance multiport-memory controller. The Version 9.2 development kit costs $495, including a MicroBlaze Version 7 processor core, an XPS (Xilinx Platform Studio) 9.2 tool suite with processing IP (intellectual-property) libraries, software drivers, documentation, and reference-design examples. XPS 9.2 supports MicroBlaze- and PowerPC-processing design for the vendor's Virtex-5, Virtex-4, Virtex-II Pro, and most Spartan-3 FPGAs. The XPS 9.2 also supports 32-bit Windows XP, SP1, SP2, 32-bit Linux Red Hat Enterprise 5.0 and 4.0, 64-bit Linux Red Hat Enterprise 5.0, and Solaris 9 (2.9/5.9). The MicroBlaze development kit, Spartan-3E 1600E edition costs $595.

Xilinx, www.xilinx.com

Development platform supports many protocols and operating systems

The MPC8360E-RDK development platform supports the EtherNet/IP and DeviceNet industrial-communication protocols. Features include graphics and touchscreen functions, a MPC8360E processor, a Linux board-support package, evaluation copies of supported industrial protocols, and evaluation copies of the Green Hills Integrity/u-Velosity RTOS (real-time operating system). The MPC8360E-RDK development platform costs $1000.

Freescale Technology, www.freescale.com

Single-core DSP runs at 1.2 GHz

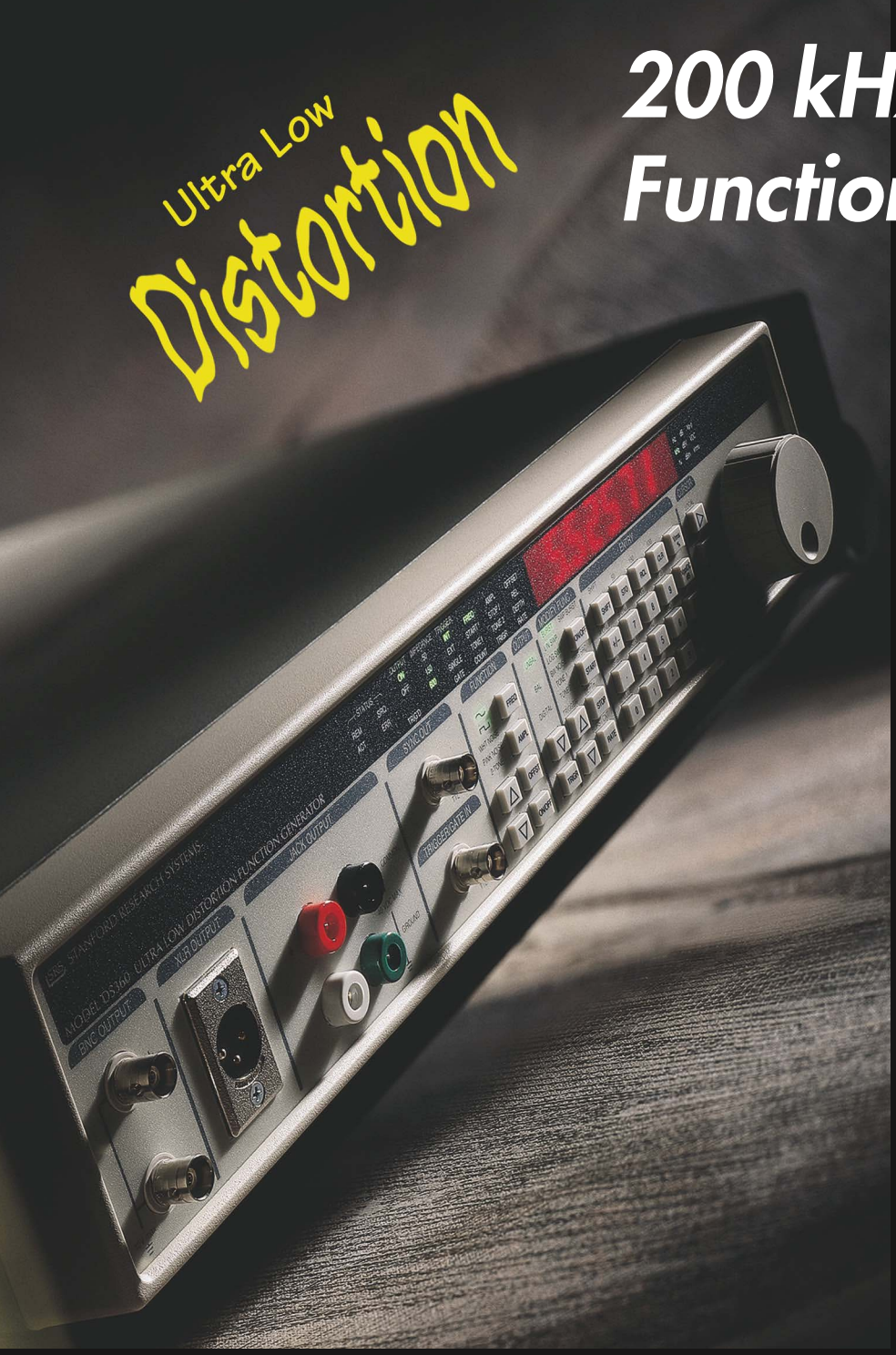
Based on the vendor's TMS320C64x+ core, the 900-MHz TMS320C6452 DSP (digital-signal processor) delivers twice the L1 cache memory and 40% more L2 cache than the C6415T. The code-compatible DSP includes two SGMII (serial-Gigabit-media-independent-interface) Ethernet MAC ports, one Gigabit switch, and a TSIP (telecom-serial-interface port). Features include a 66-MHz PCI interface, a DDR2 interface, and 32 kbytes of L1 instruction and data caches. Available in a 19×19-mm 361-lead BGA package, the 720-MHz TMS320C6452 DSP costs $96 (10,000) and the C6452 DSP evaluation module costs $1295. The 1.2-GHz TMS320C6455 DSP costs $245 (10,000), and the 1.2-GHzC6455 DSP starter kit costs $495.

Texas Instruments, www.ti.com

Compiler technology improves PSOC memory capacity

The Hi-Tech C Pro compiler technology extends memory capacity and performance of the dynamically configurable PSOC (programmable-system-on-chip) mixed-signal arrays. The device uses OCG (omniscent-code-generation) technology for examining program modules before compilation, optimizing pointers, registers, and stack allocation, as well as eliminating redundant code. In addition, the compiler frees up SRAM and reduces contention for the PSOC device's index register by compiling directly addressable function stacks for nonrecursive and nonre-entrant code. Other features include the elimination of contention in the PSOC index register, enhanced PSOC memory usage, and integration with PSOC Designer version 4.4. The C Pro compiler costs $1195 until March 2008, after which it will cost $1495. The compiler includes 12-month access to updates and technical support, as well as a 30-day money-back guarantee. A fully-functional 45-day trial version is available for download at Hi-Tech's Web site.

Hi-Tech Software, www.htsoft.com
Cypress Semiconductor, www.cypress.com



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productroundup

INTEGRATED CIRCUITS

Stereo DAC provides a variety of digital-filter options

Suiting use in high-end audio applications, the WM8741 high-performance stereo DAC delivers a 128-dB SNR (signal-to-noise ratio) in monophonic systems. Advanced digital-filter options allow users to choose between group-delay, phase-and-latency, impulse-response, and transition-band-roll-off characteristics. A low-order modulator and multibit-DAC architecture provide low out-of-band noise and world-class linearity. Additional features include interface options for both SACD (super-audio-compact-disc) and CD playback, a dithered digital-interpolation filter, and fine-resolution volume control. The converter also includes a digitally enabled de-emphasis, a multibit sigma-delta modulator, and a switched-capacitor multibit stage with differential-voltage outputs. Available in an SSOP-28 package, the DAC is a drop-in replacement for the WM8740 in some PCM (pulse-code-modulation)-mode applications. The WM8741 DAC costs $6.71 (10,000).

Wolfson Microelectronics, www.wolfsonmicro.com

Synchronous step-down converters suit low-noise operation

The AAT2120 and AA%2158 low-noise-switching-regulator family of synchronous step-down converters deliver less spectral noise, output ripple, and ringing amplitude than competing switching regulators. According to the vendor, the devices have 3 dB less spurious energy and, at higher currents, the two converters provide 25% less output ripple than competitors. The AAT2120 supplies a 500-mA output current; the AAT2158 delivers a 1.5A output current. Both devices have a 2.7 to 5.5V operating current, support 0.6V output voltages, and have a −40 to +85°C temperature range. The converters provide internal soft-start, overtemperature, and current-limit protection, as well as extended system runtime by adding 100%-duty-cycle, low-dropout operation. Available in a 2×2-mm STDFN-8 package, the AAT2120 costs 85 cents (1000); the AAT2158 comes in a 3×3-mm QFN-16 package and costs $1.55 (1000).

Advanced Analogic Technologies, www.analogictech.com

DAC combines user-programmable current source and voltage output

Integrating current-source and voltage-output DACs, the precision AD5422 converter suits use in factory-process control, distributed control, and smart-transmitter systems. Using iCMOS industrial-process technology, the 16-bit single-channel converter operates from a 12 to 48V supply or dual ±12 to ±24V supplies. A software-selectable output configuration provides 5, 10, ±5, and ±10V voltage-mode options and 0- to 20-, 4- to 20-, and 0- to 24-mA current-mode options, with output spans including an additional overrange setting. Claiming a 0.1% total-unadjusted-error accuracy level, the converter provides a precision 5-ppm/°C internal reference. Internal fault-detection circuitry provides hardware and software indication of line faults, such as opens or shorts in cable wiring or remotely located loads. Additional features include a buffered voltage output with force and sense capabilities, an output amplifier allowing rail-to-rail output swing, and analog outputs driving 1-µF capacitive loads and 1H inductive loads. The device supports a 30-MHz SPI (serial-peripheral interface), power-on reset, and an industrial-temperature range. Available in TSSOP-24 and LFCSP-40 packages, the AD5422 costs $4.95.

Analog Devices, www.analog.com

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LOOKING AHEAD

TO ISSCC 2008

The ISSCC (International Solid-State Circuits Conference), the foremost annual technical conference for leading-edge-IC developments, runs from Feb 3 to 7, 2008, in San Francisco. As always, the conference will include papers on new ICs and circuits in areas ranging from memory, processors, and communications to the latest in integrated digital radios and networking devices. Papers will also cover advanced circuit designs to push the envelope on performance in a given technology, as well as analog- and data-conversion circuits. This year's theme, "system integration for life and style," should attract a plethora of papers on advanced consumer ICs, personal-area networks, and sensors for the rapidly emerging area of bio-electronic systems. Watch for the advanced technology sessions, during which sparks can fly.

LOOKING BACK

AT ADVANCES IN EMBEDDED COMPUTING

A newly developed digital airborne computer performs all computations for navigation, fire control, bombing, and weapons control at the speeds necessary for modern weapons systems. Designer and builder Ramo-Wooldridge says the unit can conduct 4000 complete arithmetic operations per second—including access time—and requires only 400W for operation. The airborne system comprises four units: a magnetic-drum-storage unit, an arithmetic-and-control unit, an input-output unit, and a clock/power unit. Silicon semiconductors and subminiaturized packaging permit the unit to occupy only 4.19 cubic feet and weigh 203 pounds.

—*Electrical Design News*, December 1957

LOOKING AROUND

AT TAIWAN AS AN EMERGING CHIP-DESIGN POWERHOUSE

It's easy to stereotype Taiwan as a fine, if expensive, place to outsource chip design for a mature design project. But most view the country as not ready for the big leagues. That perception is an increasingly dangerous underestimatation of the rapidly growing design sophistication in Taiwan. For example, TSMC (Taiwan Semiconductor Manufacturing Co, www.tsmc.com) is quietly expanding its design expertise beyond traditional foundry responsibilities to complex intellectual-property blocks and complete design flows. Following in TSMC's footsteps, Taiwanese chip-design teams are morphing from contract-design shops into full fabless-semiconductor companies, in some cases able to handle leading-edge designs. Recent data from Synopsys (www.synopsys.com) suggests that many Taiwanese teams are now comfortable working with 90-nm processes, and a few 45-nm designs there are under way.

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